

LCFC Confidential


BMWD1 M/B Schematics Document

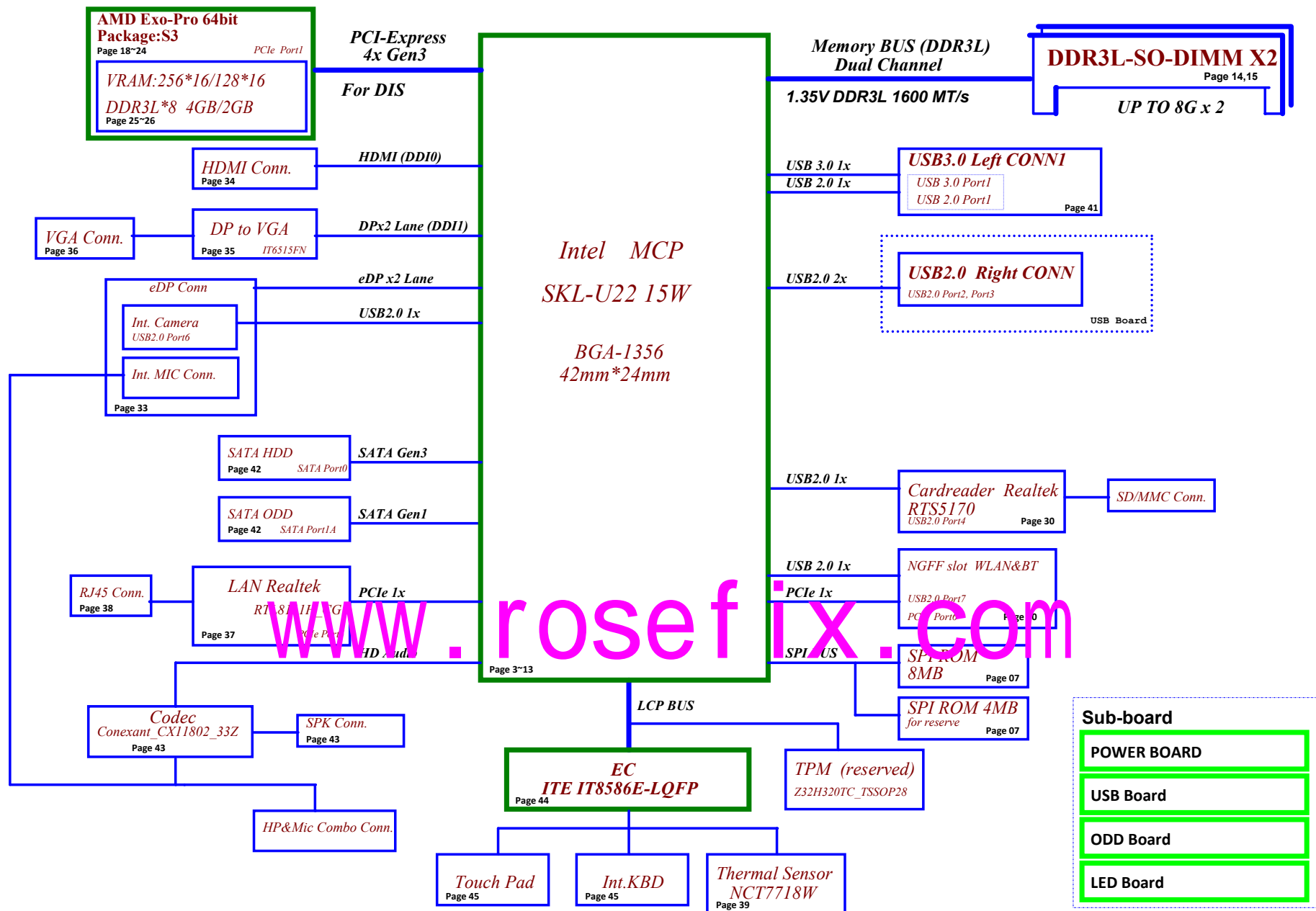
Intel Skylake U22 with DDRIII L + AMD Exo-Pro-S3 GPU

2015-08-10

REV:1.0

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Security Classification	LC Future Center Secret Data			Title		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.35V +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.675VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1 USB3.0 CONN left	@	Not stuff
	2 NC	14@	For 14" part
	3 NC	15@	For 15" part
	4 NC	14or15@	For 14" or 15" part
	5 NC	14or17@	For 14" or 17" part
	6 NC	AOAC@	AOAC support part
USB2.0	1 USB3.0 CONN Left	BCD@	For C cost down (BDW)
	2 USB2.0 CONN1 Right	Cannonlake@	For Cannonlake part
	3 USB2.0 CONN2 Right	CD@	For C cost down
	4 Camera	DUALMIC@	For Dual MIC part
	5 Cardreader	EMC@	For EMC part
	6 Touch Panel	EMC_15@	For EMC 15" part
	7 BT	EMC_NS@	For EMC nu-stuff part
	8 NC	EMC_PX@	For EMC PX part
	9 NC	EMC_PXNS@	For EMC PX nu-stuff part
	10 NC	ES@	For ES CPU
PCIe	1 NC	EXO@	For EXO GPU
	2 NC	GCLK@	For GreenCLK part
	3 NC	ME@	For ME part
	4 NC	NTS@	For nu-touch part
	5 LAN	PCH_SDIO@	For PCH SDIO part
	6 WLAN	PCH_SDIO1@	For PCH SDIO path1
	7 used as SATA	PCH_SDIO2@	For PCH SDIO path2
	8 used as SATA	PX@	For PX part
	9 X4 PCIe (9-12)	RANKA@	For VRAM rank A part
	10 DGPU	RANKB@	For VRAM rank B part
SATA	0 HDD	Realtek_SD@	For Realtek SD part
	1A ODD	SINGLEMIC@	For single MIC part
	1B used as PCIe	SINGLERANK@	For single VRAM rank part
	2 used as PCIe	DUALRANK@	For dual VRAM rank part
		TS@	For touch screen part
		TPM@	For TPM part
		UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger	DGPU
EC_SMB_CK1	IT8586E	V	V	X	X	X	X	X	V	X
EC_SMB_DA1	+3VALW	V	+3VALW	X	X	X	X	X	V	X
EC_SMB_CK2	IT8586E	X	V	X	X	V	V	X	X	V
EC_SMB_DA2	+3VS	X	+3VS	X	X	+3VS	+3VALW_PCH	X	X	+3VGS
PCH_SMB_CLK	PCH	X	X	V	V	X	V	X	X	X
PCH_SMB_DATA	+3VALW_PCH	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X	X

EC SM Bus1 address

EC SM Bus2 address

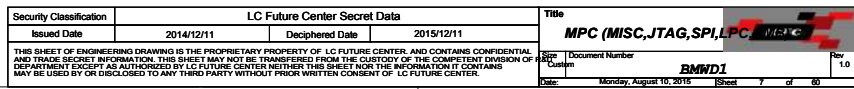
PCH SM Bus address

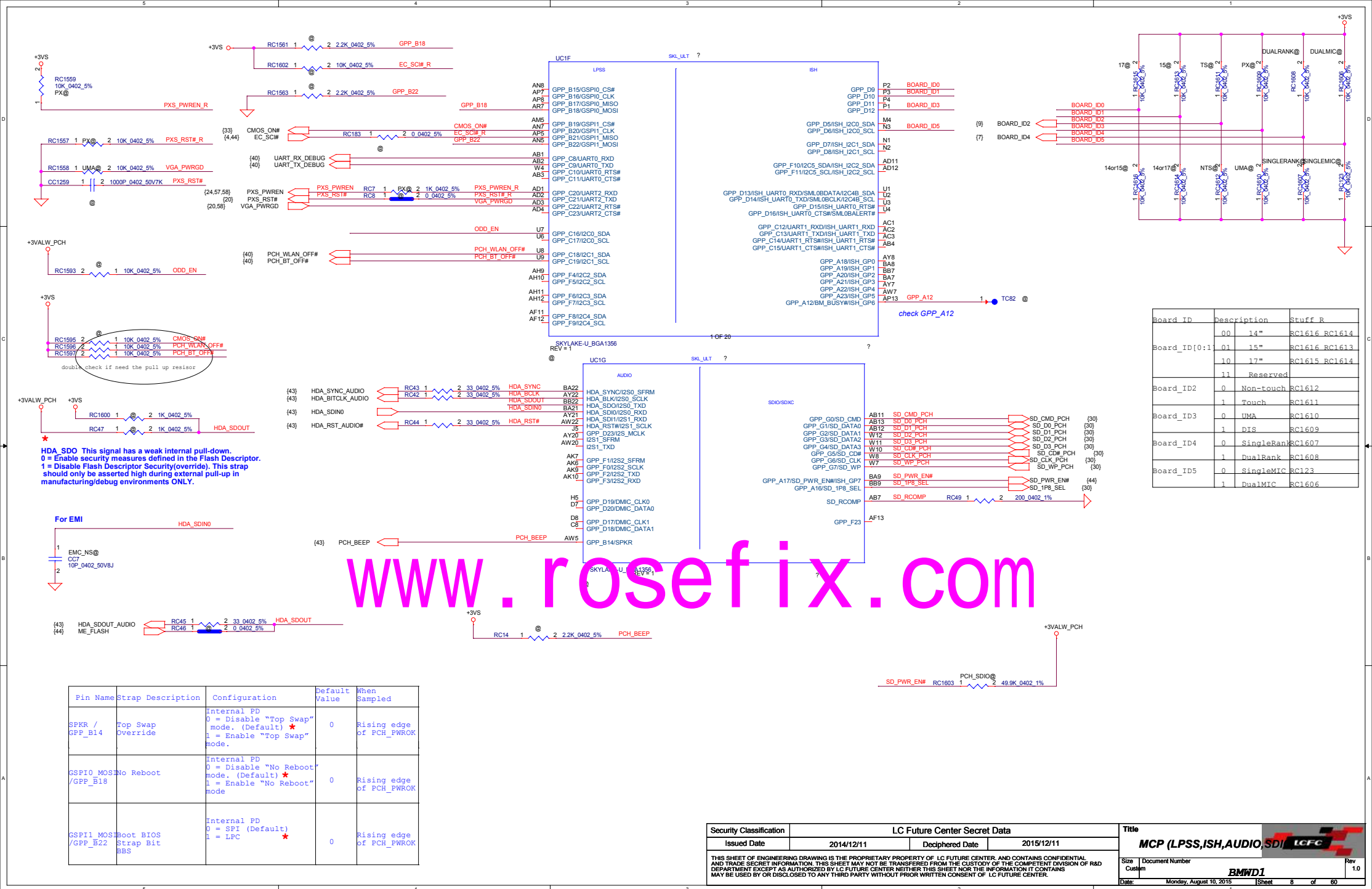
Device	Address
Smart Battery	0X16
Charger	0001 0010 b

Device	Address
Thermal Sensor NCT7718W	1001_100xb
PCH	need to update
DGPU	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

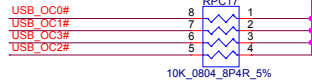
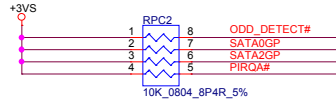
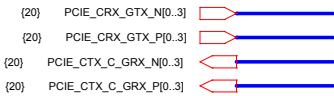
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third-part dGPU PCIEP9

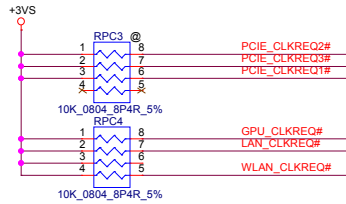
PCIE RCOMP and PCIE RCOMP
Trace Width: 12-15mil
Differential between RCOMP/RCOMP



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Title		MCP (PCIE,SATA,USB3,US	
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check the Pull up resistor

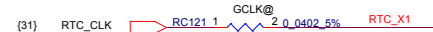
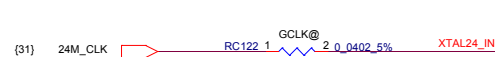
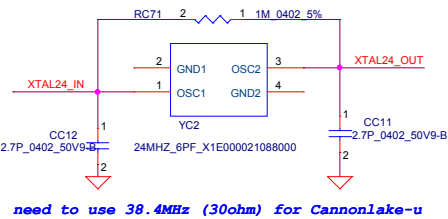


PCIE CLK0 GPU

PCIE CLK5 LAN

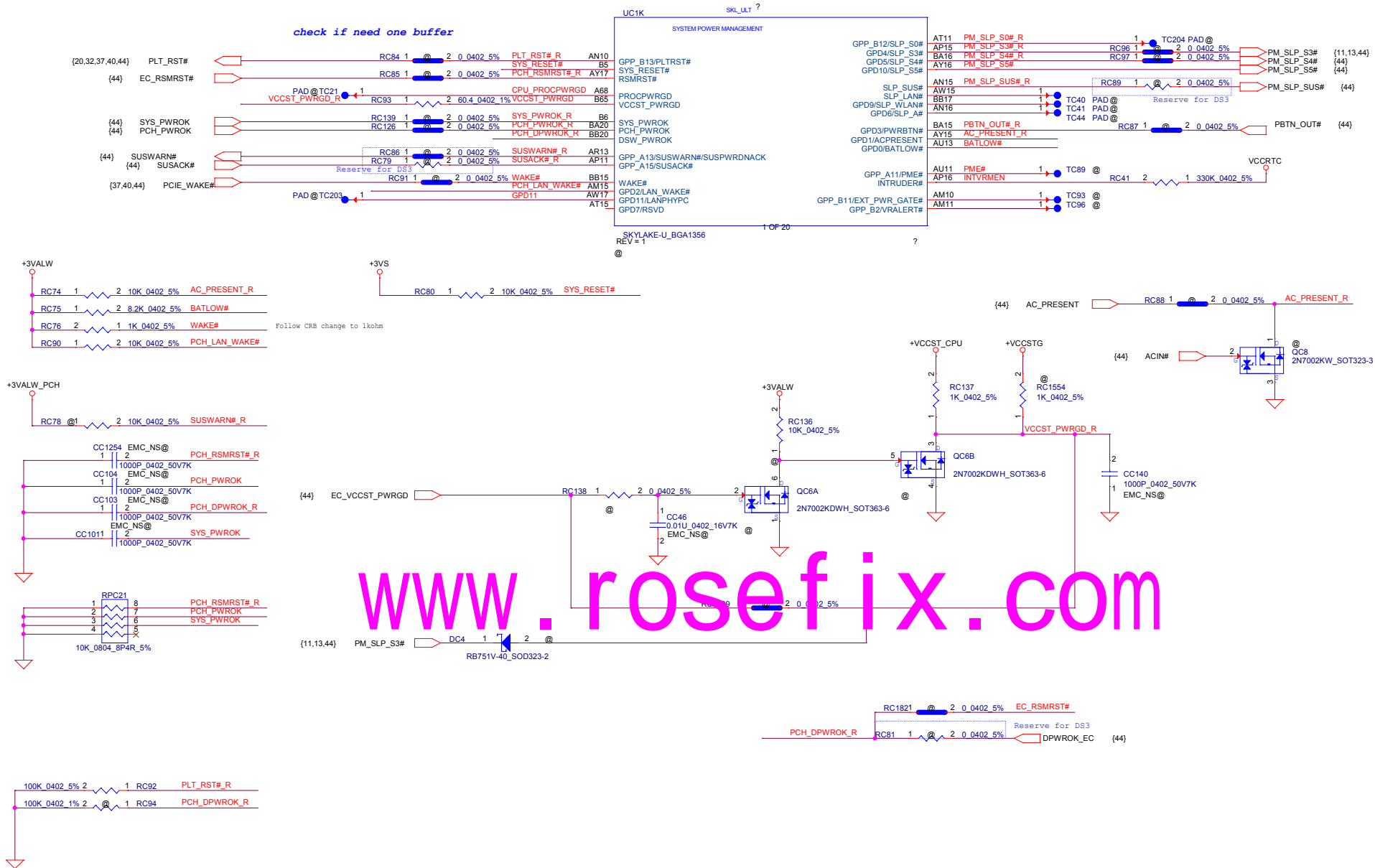
PCIE CLK6 WLAN


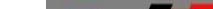
check if need to change to 1M_0402_1% follow PDG, CRB is 1M_0402_5%

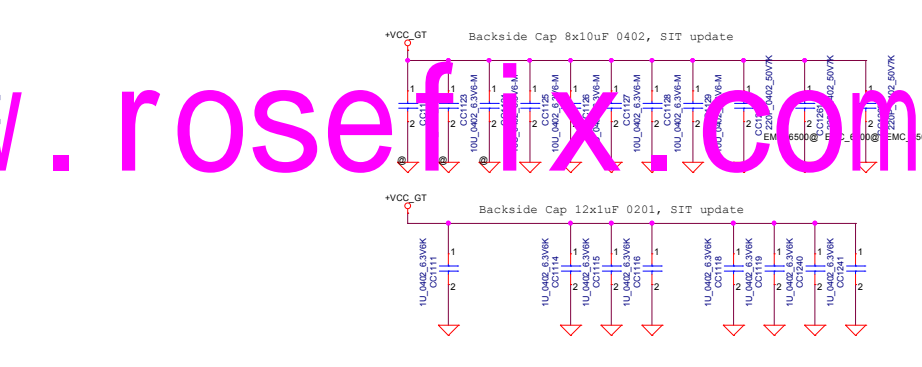
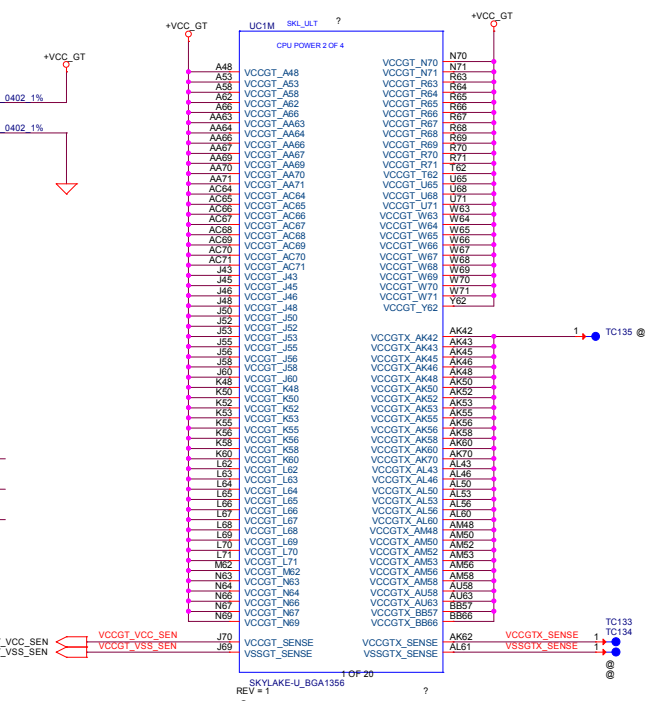



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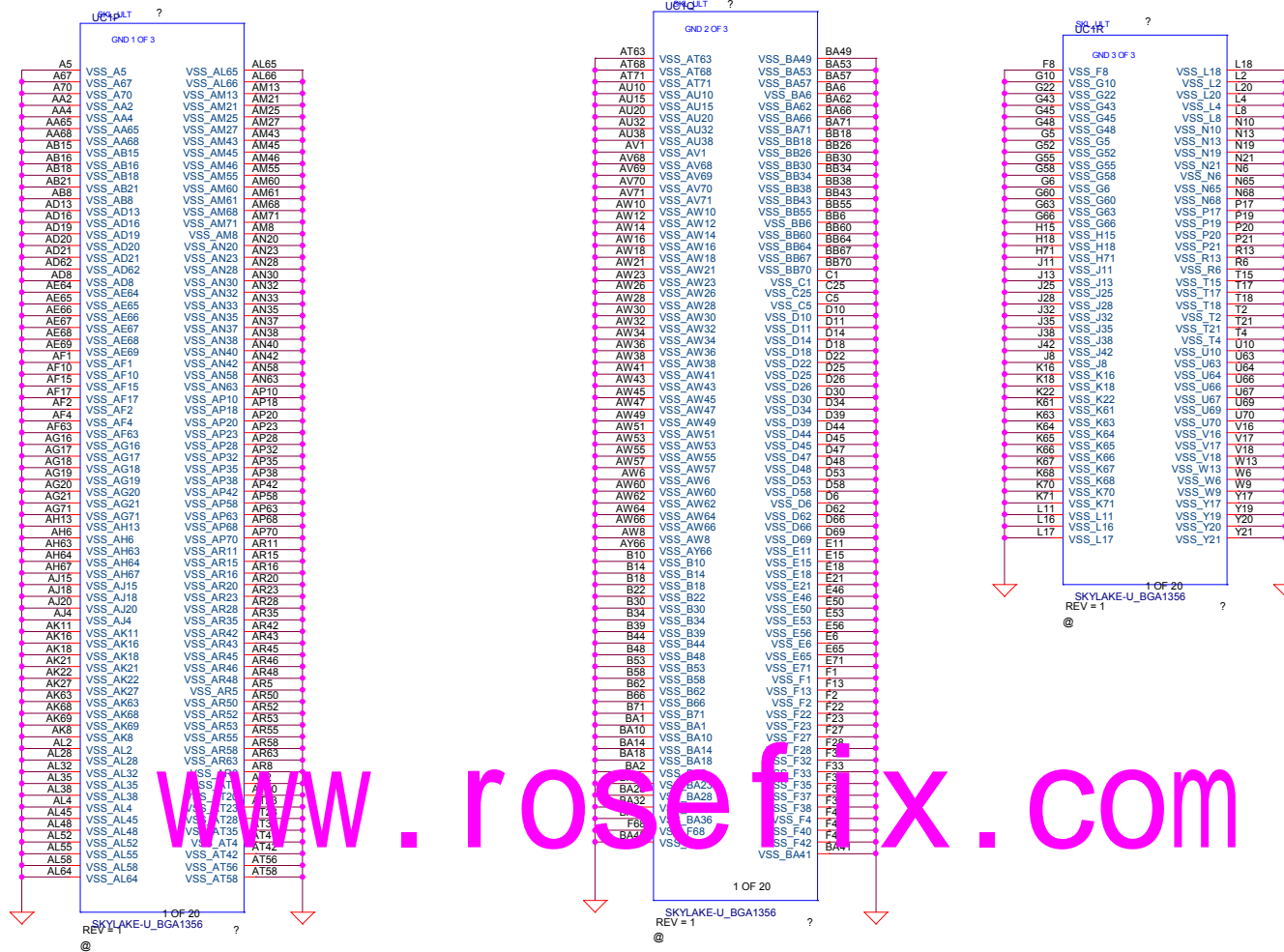
check if need one buffer

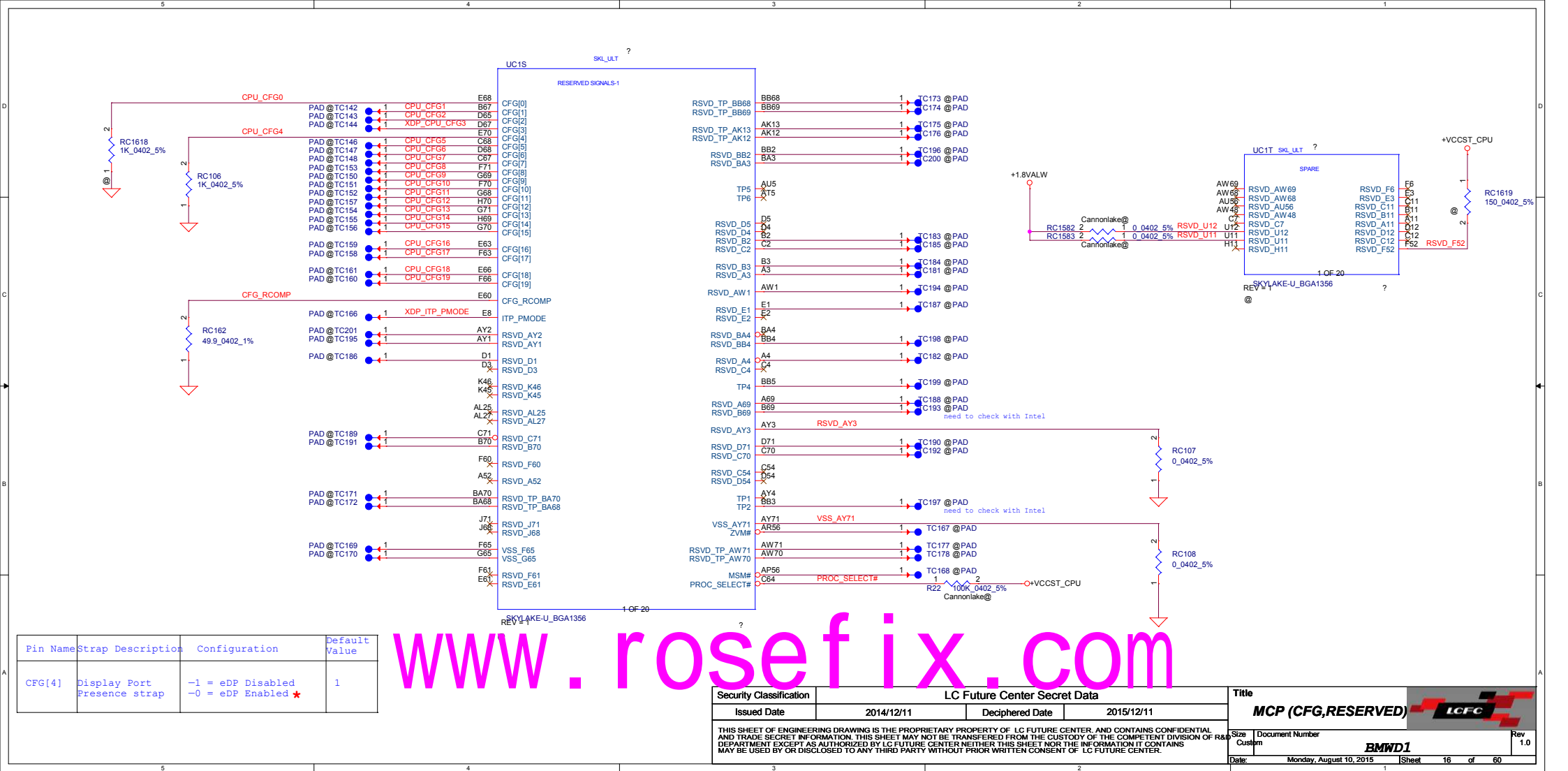


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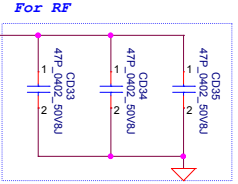
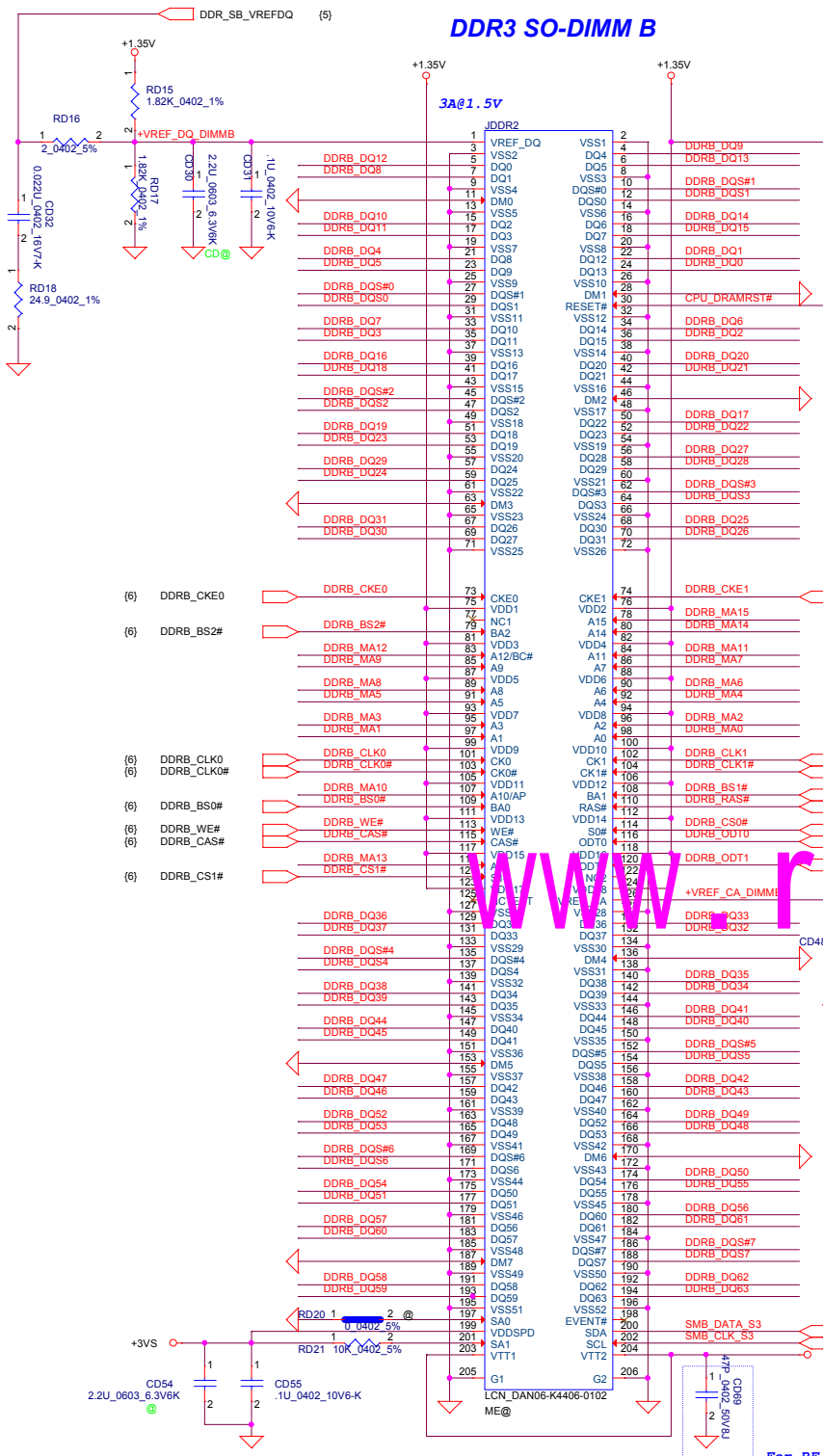


Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	-1 = eDP Disabled -0 = eDP Enabled ★	1

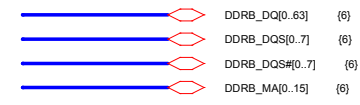
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DDR3 SO-DIMM B



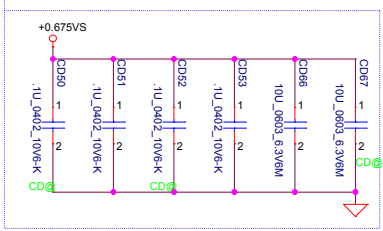
Layout Note:
Place near DIMM



Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR_B_DQ12
7	DQ2	DDR_B_DQ8
15	DQ1	DDR_B_DQ10
17	DQ3	DDR_B_DQ11
4	DQ4	DDR_B_DQ9
6	DQ5	DDR_B_DQ13
16	DQ6	DDR_B_DQ14
18	DQ7	DDR_B_DQ15
10	DQS#0	DDR_B_DQS#1
12	DQS0	DDR_B_DQS1
21	DQ8	DDR_B_DQ4
23	DQ9	DDR_B_DQ5
33	DQ10	DDR_B_DQ7
35	DQ11	DDR_B_DQ3
22	DQ12	DDR_B_DQ1
24	DQ13	DDR_B_DQ0
34	DQ14	DDR_B_DQ6
36	DQ15	DDR_B_DQ2
27	DQS#1	DDR_B_DQS#0
29	DQS1	DDR_B_DQS0
39	DQ16	DDR_B_DQ16
41	DQ17	DDR_B_DQ18
51	DQ18	DDR_B_DQ19
53	DQ19	DDR_B_DQ23
40	DQ20	DDR_B_DQ20
42	DQ21	DDR_B_DQ21
50	DQ22	DDR_B_DQ17
52	DQ23	DDR_B_DQ22
45	DQS#2	DDR_B_DQS#2
47	DQS2	DDR_B_DQS2
57	DQ24	DDR_B_DQ29
59	DQ25	DDR_B_DQ24
67	DQ26	DDR_B_DQ31
69	DQ27	DDR_B_DQ30
56	DQ28	DDR_B_DQ27
58	DQ29	DDR_B_DQ28
68	DQ30	DDR_B_DQ25
70	DQ31	DDR_B_DQ26
62	DQS#3	DDR_B_DQS#3
64	DQS3	DDR_B_DQS3
129	DQ32	DDR_B_DQ36
131	DQ33	DDR_B_DQ37
141	DQ34	DDR_B_DQ38
143	DQ35	DDR_B_DQ39
130	DQ36	DDR_B_DQ33
132	DQ37	DDR_B_DQ32
140	DQ38	DDR_B_DQ35
142	DQ39	DDR_B_DQ34
135	DQS#4	DDR_B_DQS#4
137	DQS4	DDR_B_DQS4
147	DQ40	DDR_B_DQ44
149	DQ41	DDR_B_DQ45
157	DQ42	DDR_B_DQ47
159	DQ43	DDR_B_DQ46
146	DQ44	DDR_B_DQ41
148	DQ45	DDR_B_DQ40
158	DQ46	DDR_B_DQ42
160	DQ47	DDR_B_DQ43
152	DQS#5	DDR_B_DQS#5
154	DQS5	DDR_B_DQS5
163	DQ48	DDR_B_DQ52
165	DQ49	DDR_B_DQ53
175	DQ50	DDR_B_DQ54
177	DQ51	DDR_B_DQ51
164	DQ52	DDR_B_DQ49
166	DQ53	DDR_B_DQ48
174	DQ54	DDR_B_DQ50
176	DQ55	DDR_B_DQ55
168	DQS#6	DDR_B_DQS#6
171	DQS6	DDR_B_DQS6
181	DQ56	DDR_B_DQ57
183	DQ57	DDR_B_DQ60
191	DQ58	DDR_B_DQ58
193	DQ59	DDR_B_DQ59
180	DQ60	DDR_B_DQ56
182	DQ61	DDR_B_DQ61
192	DQ62	DDR_B_DQ62
194	DQ63	DDR_B_DQ63
186	DQS#7	DDR_B_DQS#7
188	DQS7	DDR_B_DQS7

Layout Note:
Place near DIMM



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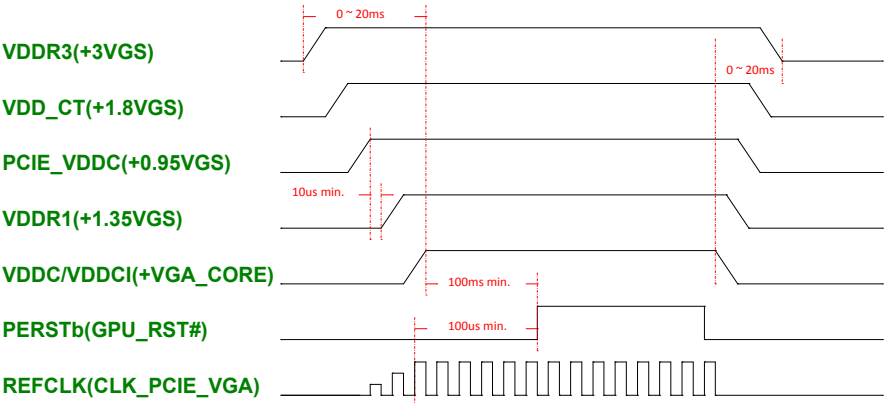
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1.0

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs. It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs). For power down, reversing the ramp-up sequence is recommended.



CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE			
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16J-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C (New)	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646E-BC1A (New no AVL)	001	8.45K	2K

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VGA Notes List

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Sheet

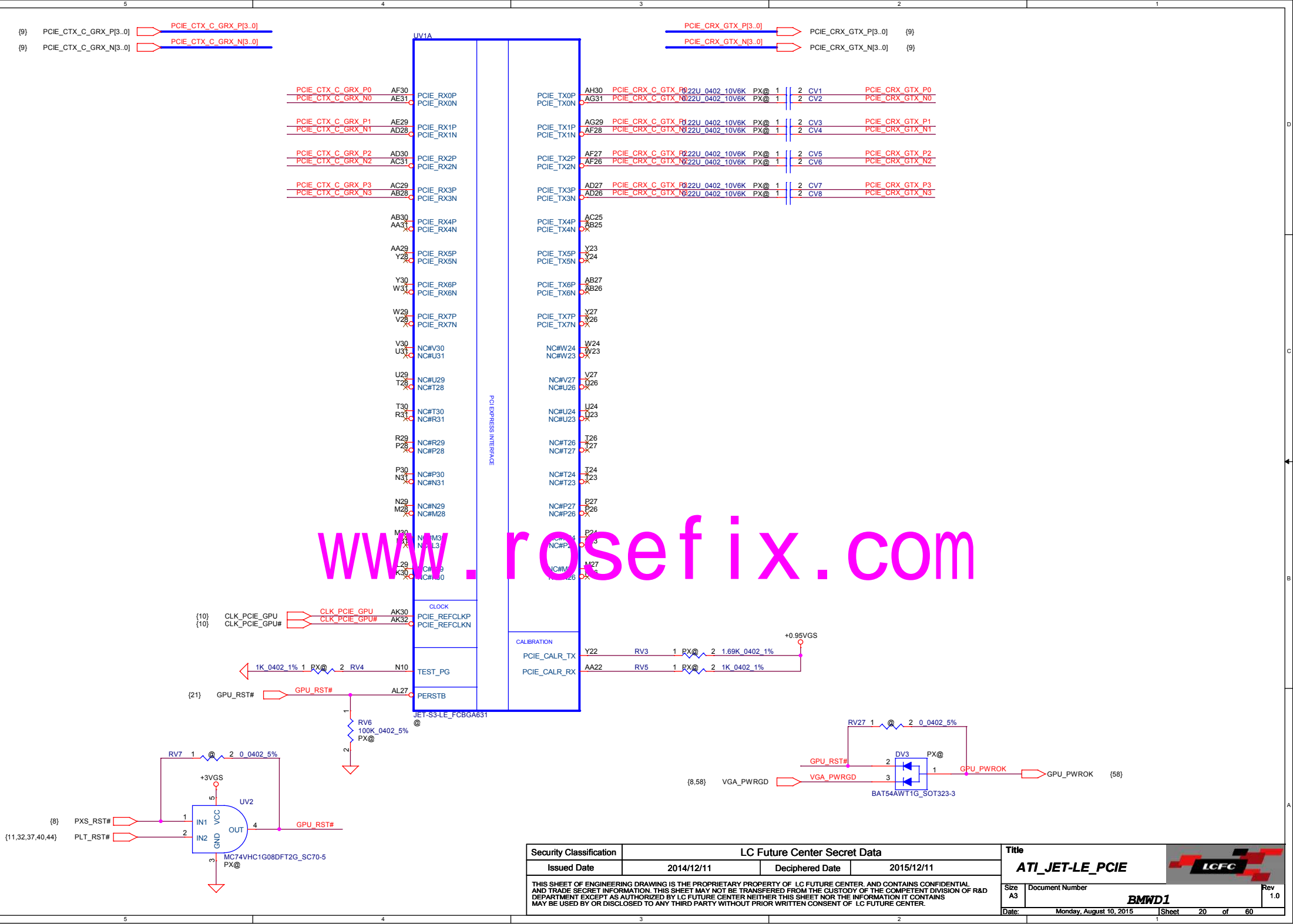
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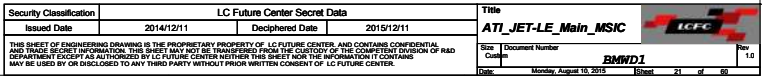
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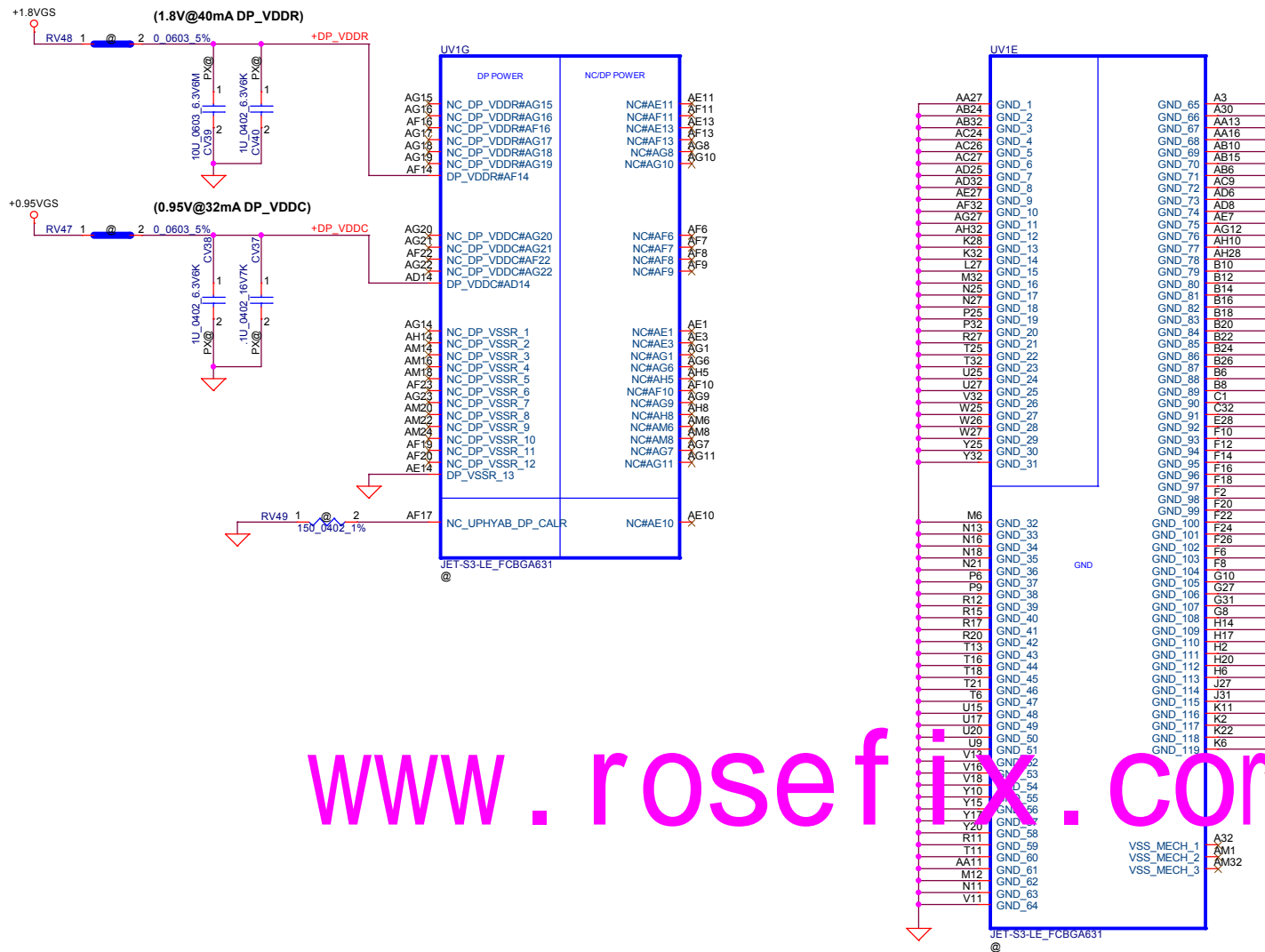
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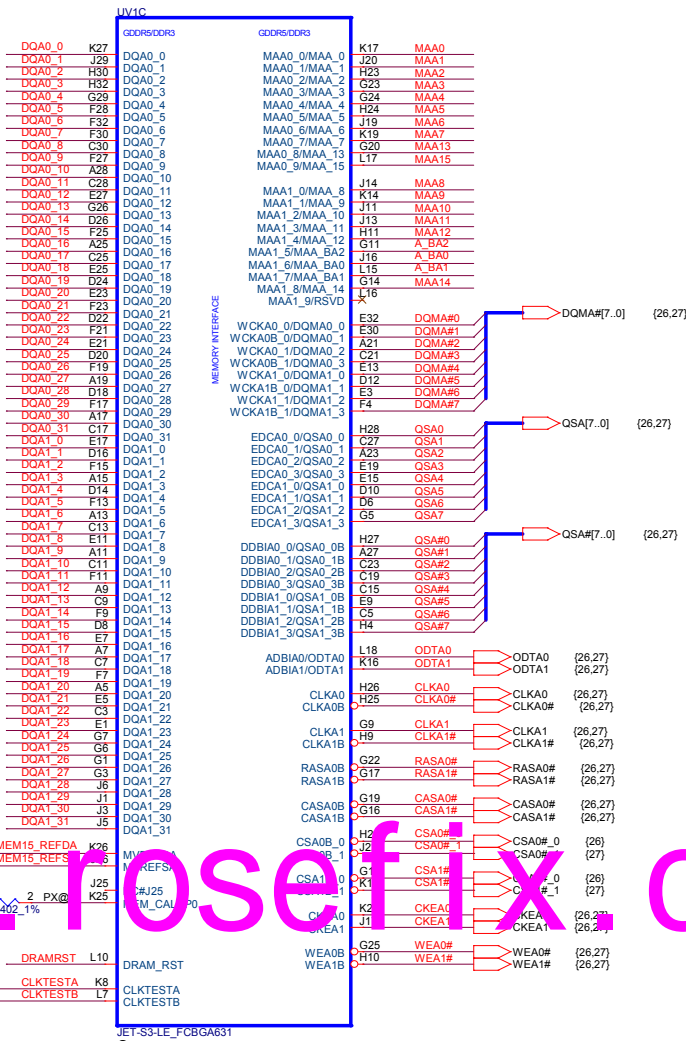
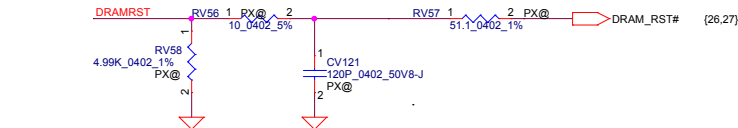
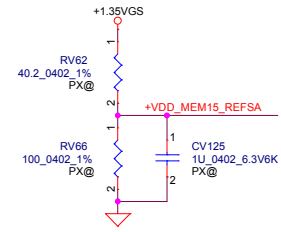
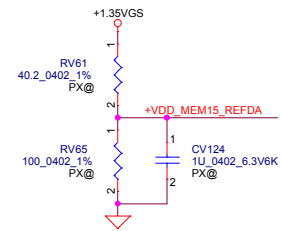
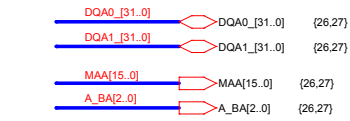


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				Date: Monday, August 10, 2015	Sheet 22 of 60

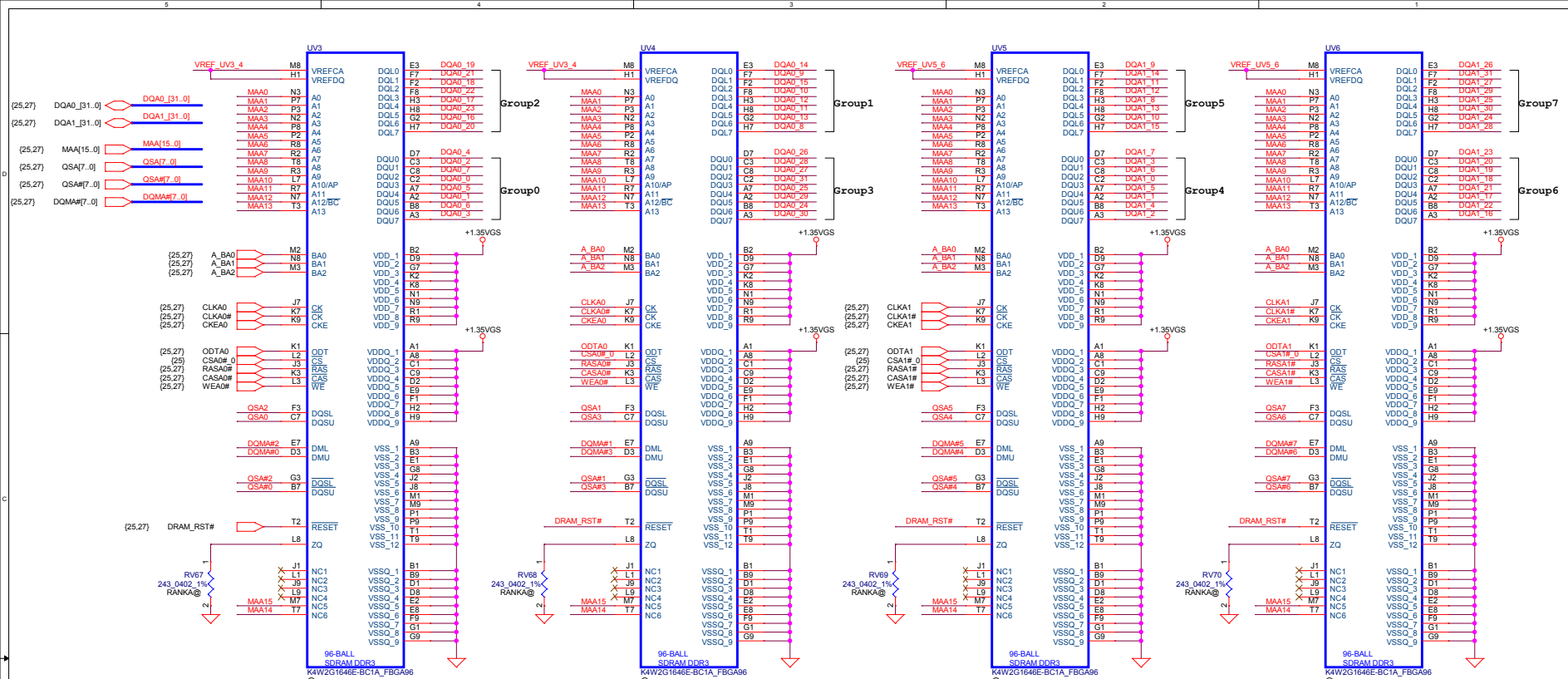


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						Custom	BMWD1		
Date:		Monday, August 10, 2015		Sheet		23	of	60	

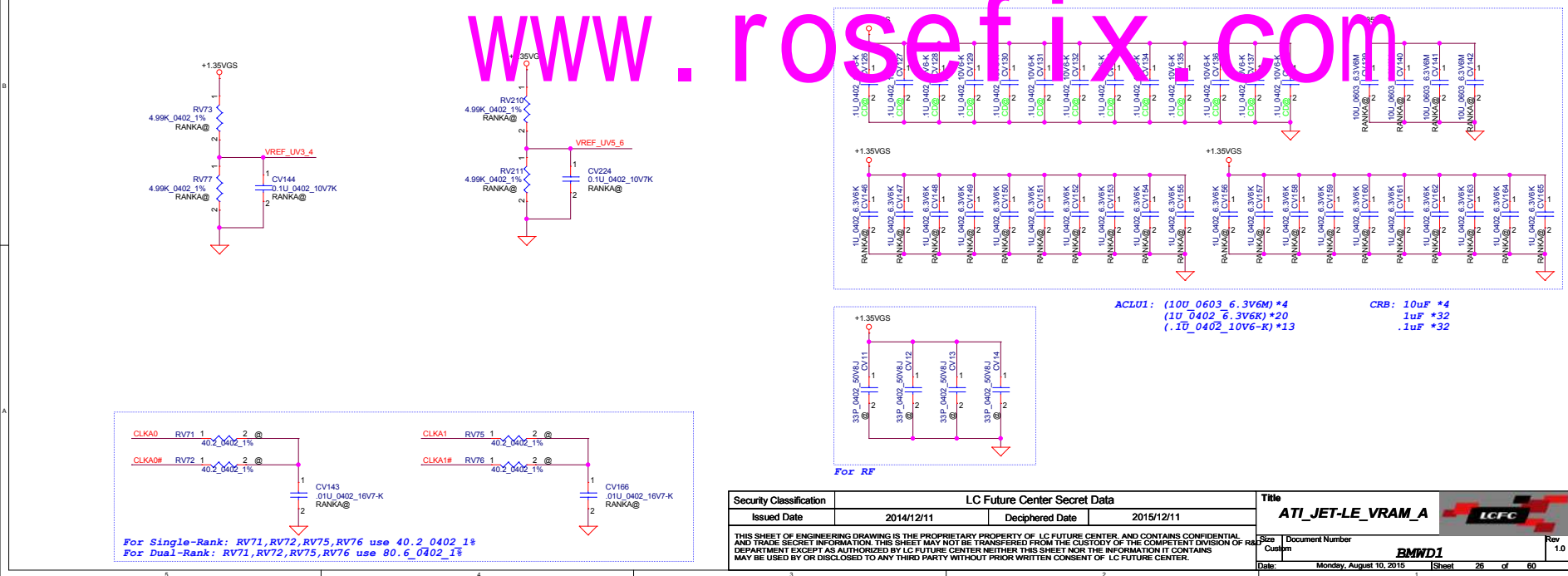


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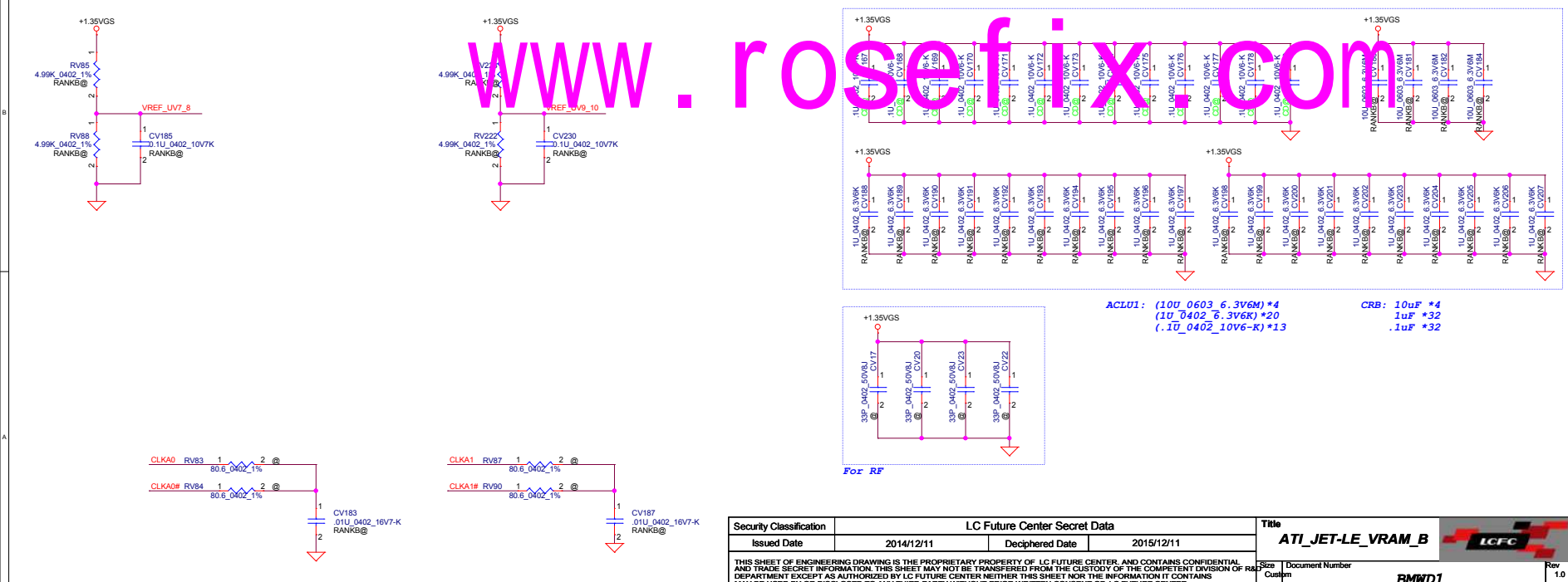
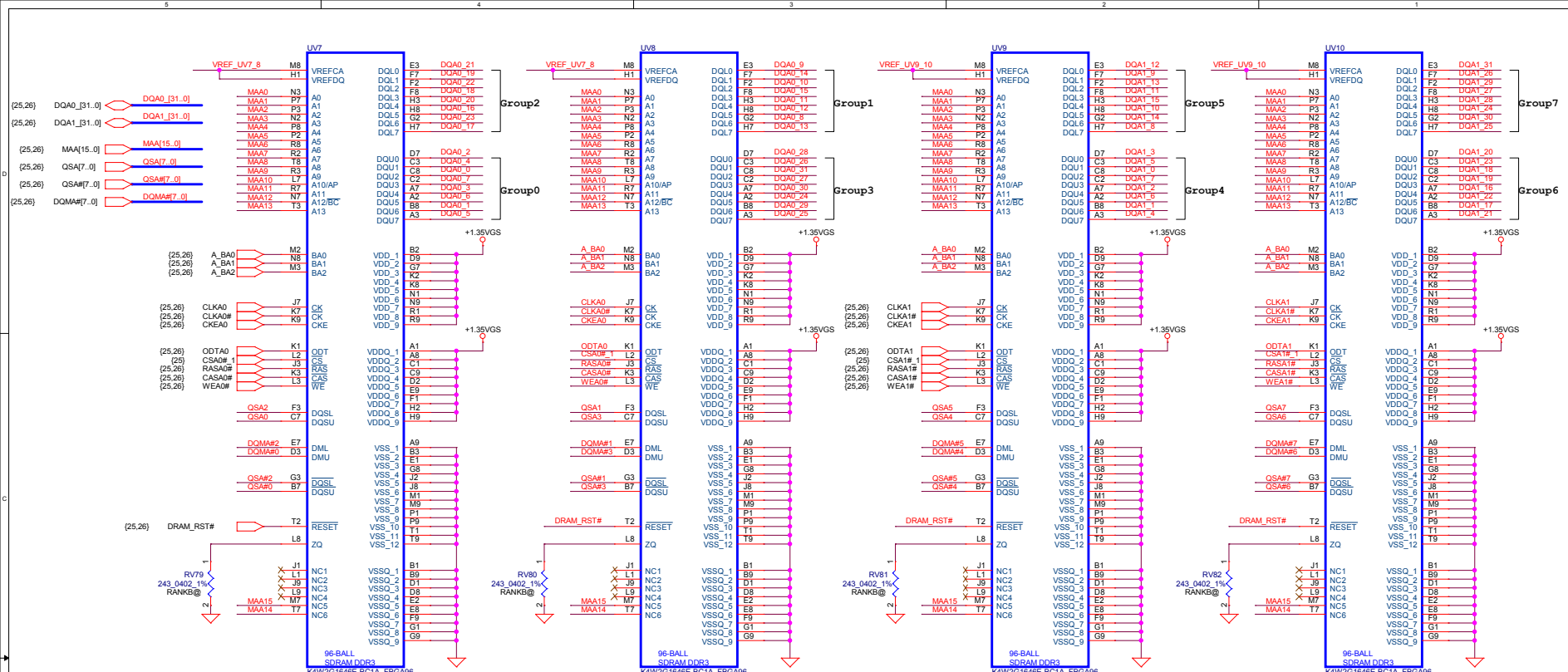
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Custom		BMWD1							
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				Document Number	1.0
				BMWD1	
Date:		Monday, August 10, 2015		Sheet 26 of 60	

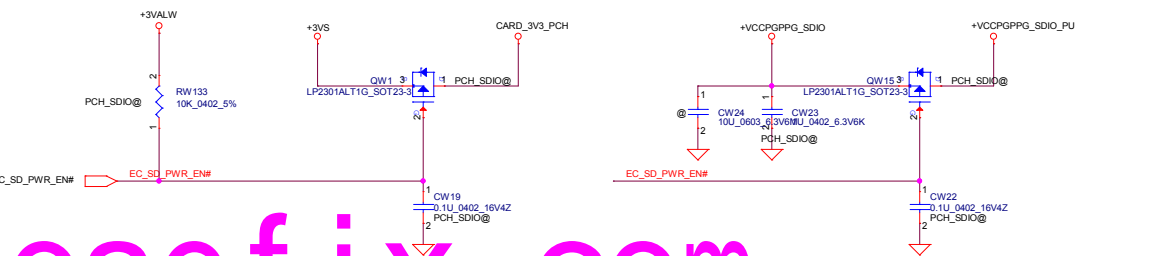
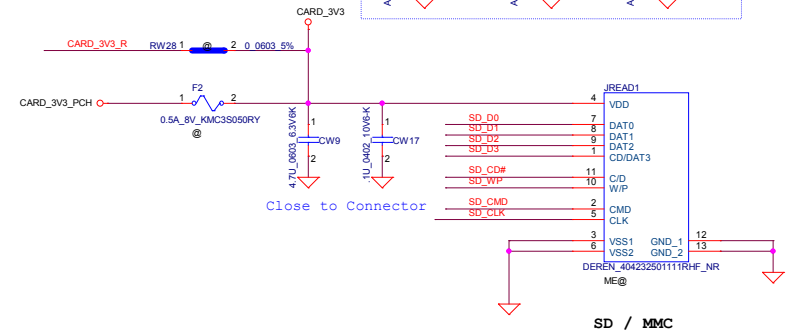
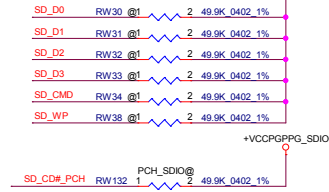
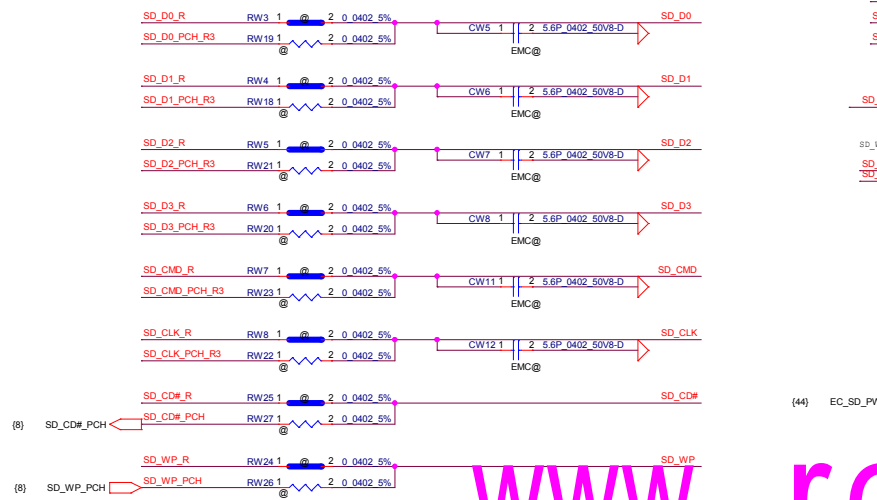
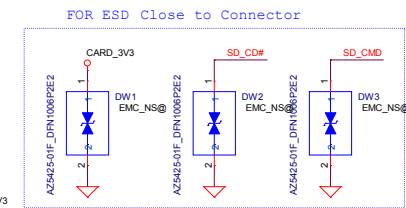
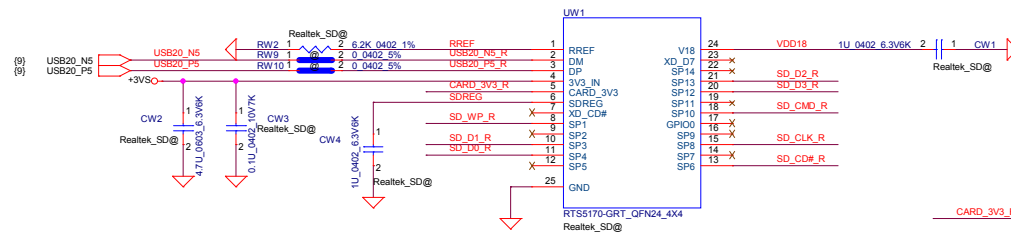
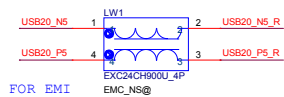


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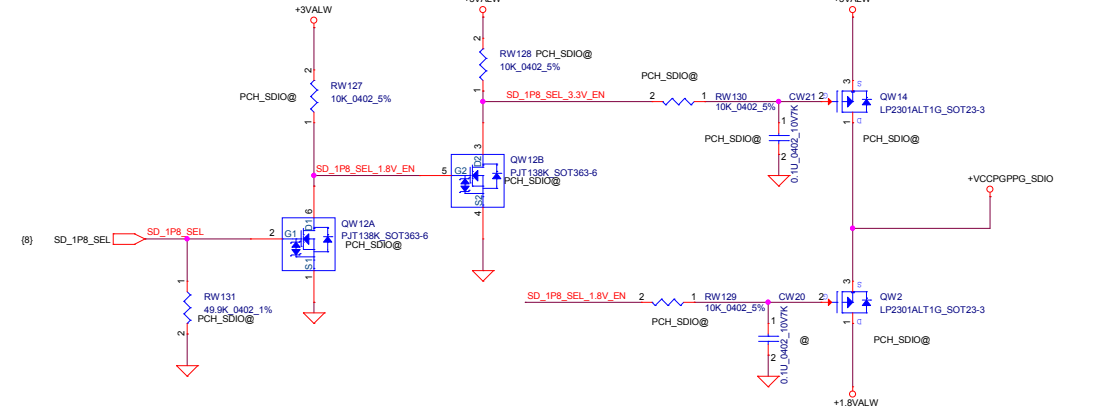
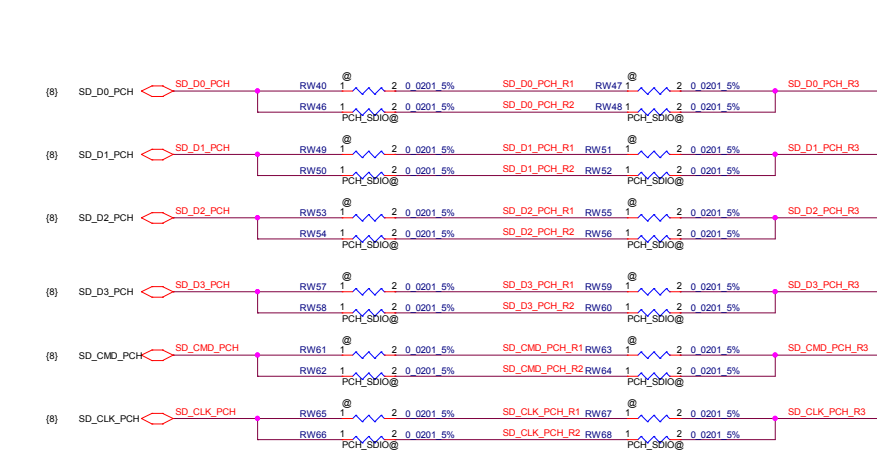
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				Date:	Monday, August 10, 2015	Sheet	28 of 60

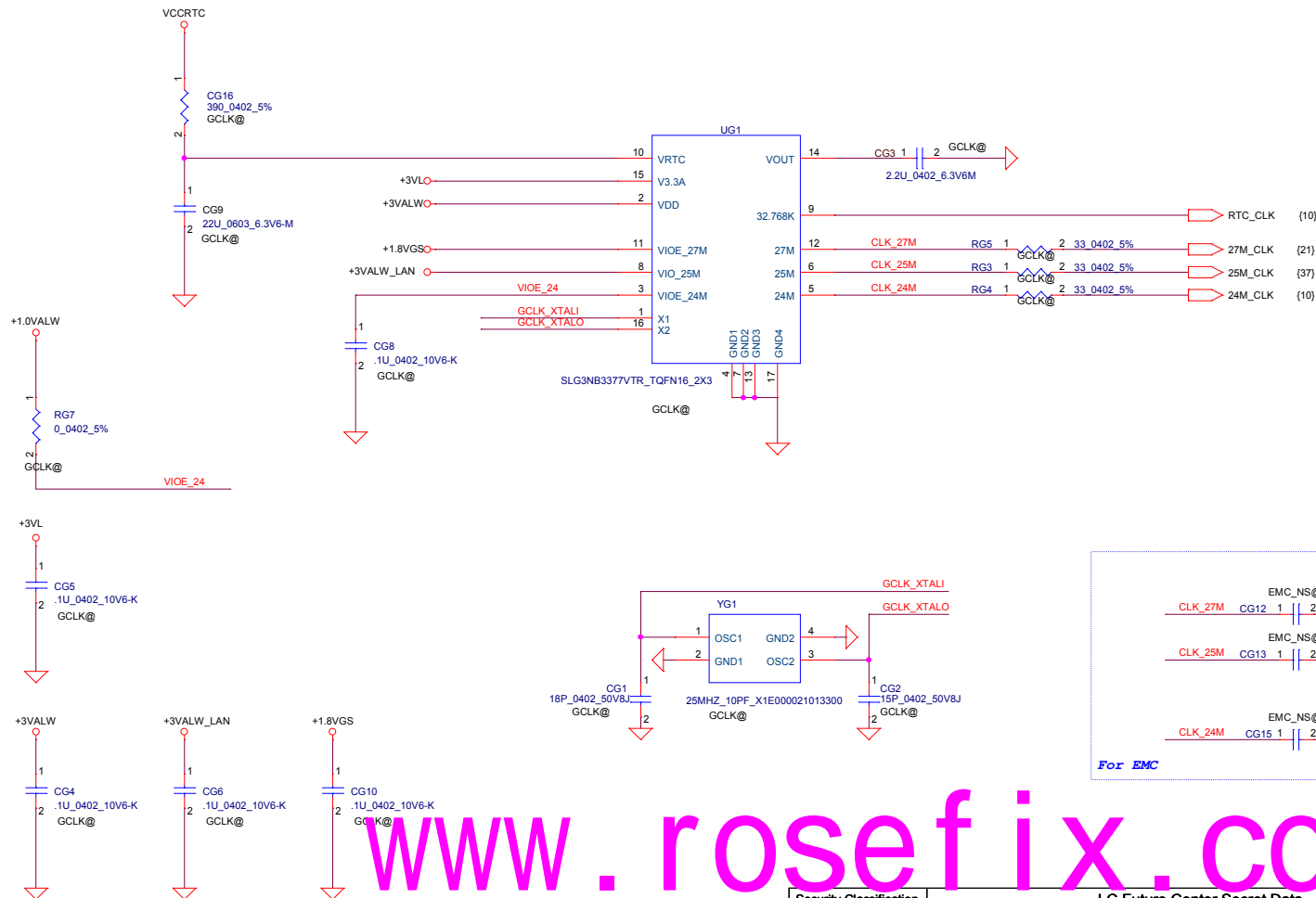
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Size		Document Number		Rev			
Custom		BMWD1		1.0			
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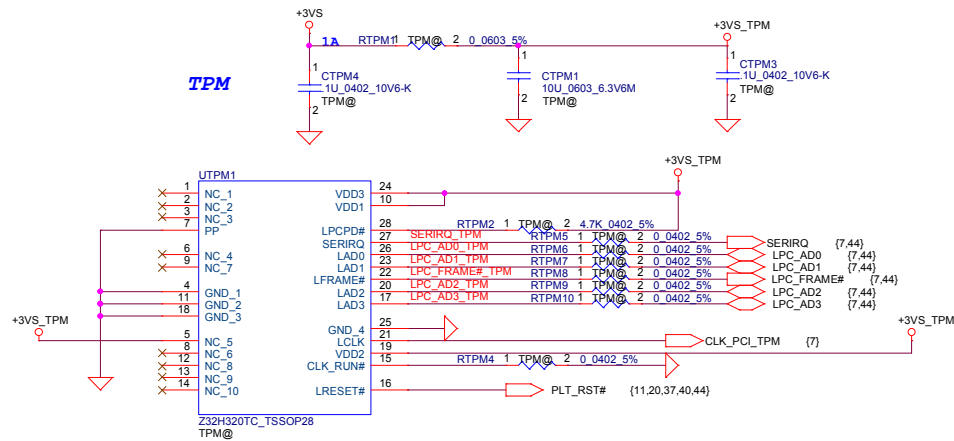
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					Custom	Document Number
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					Date: Monday, August 10, 2015	Sheet 31 of 60

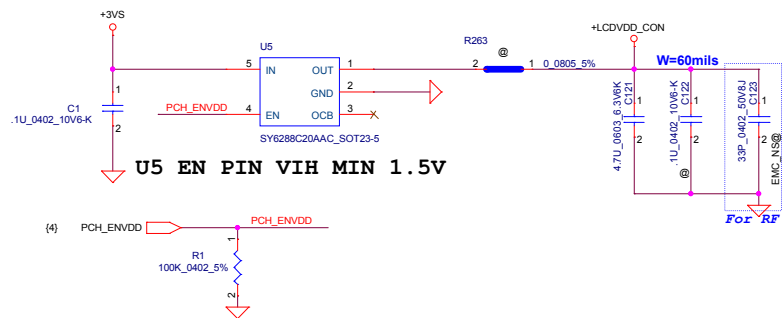


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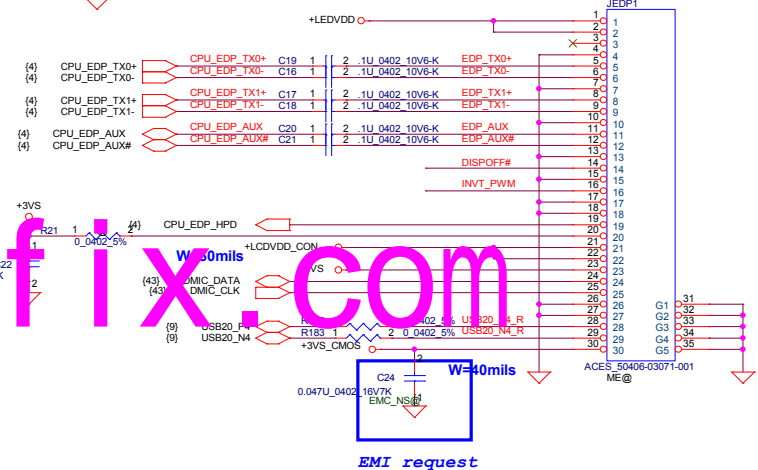
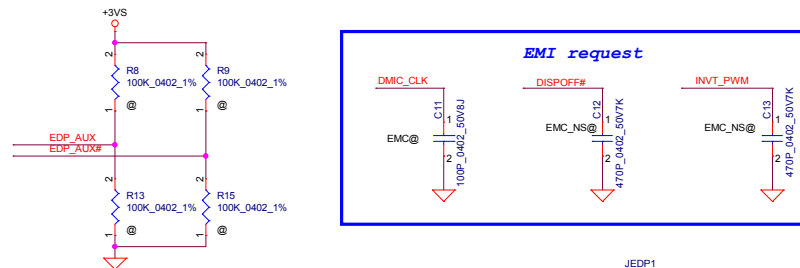
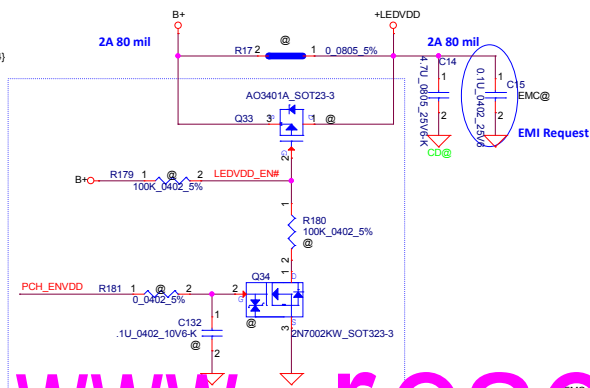
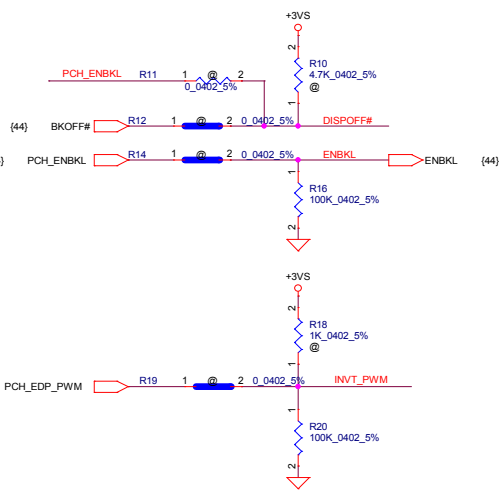
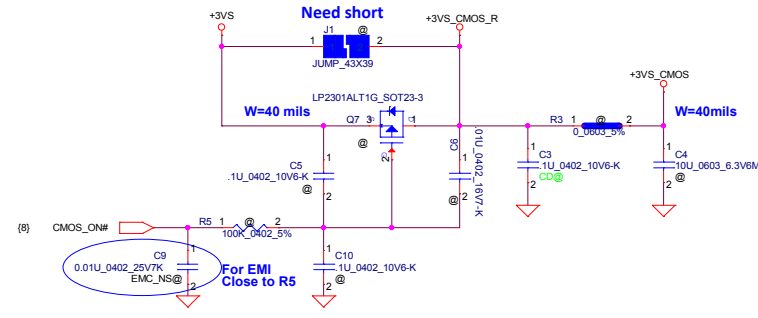
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				Date	Monday, August 10, 2015
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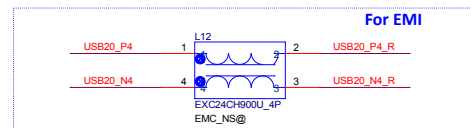
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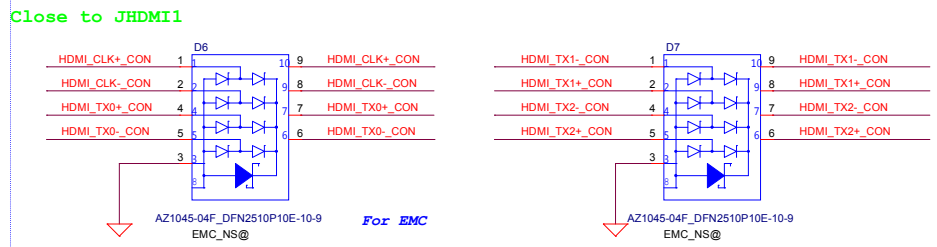
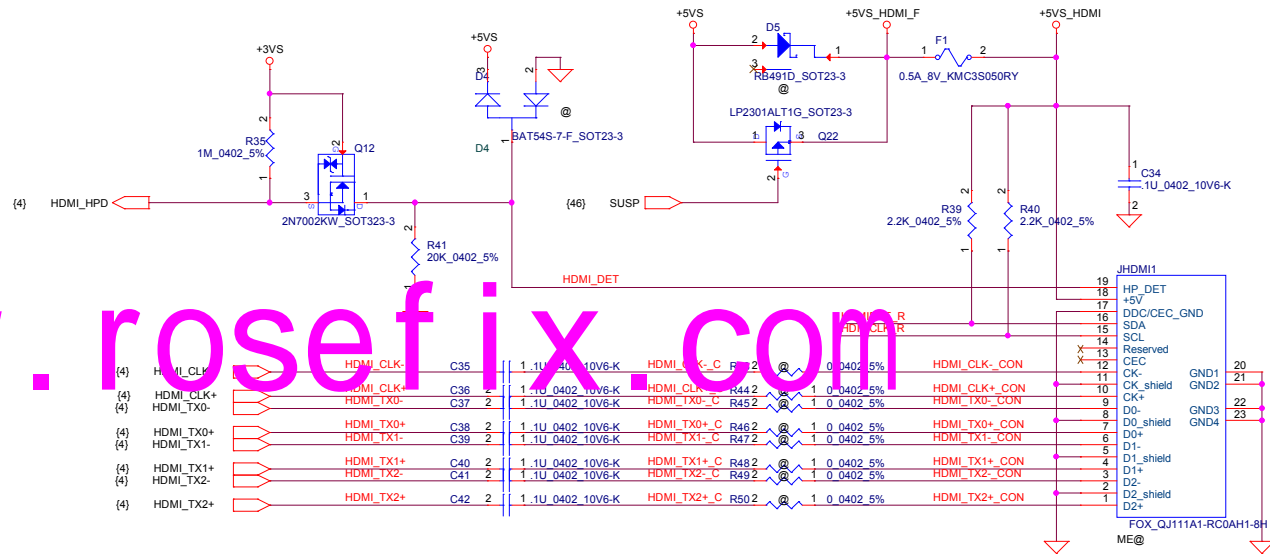
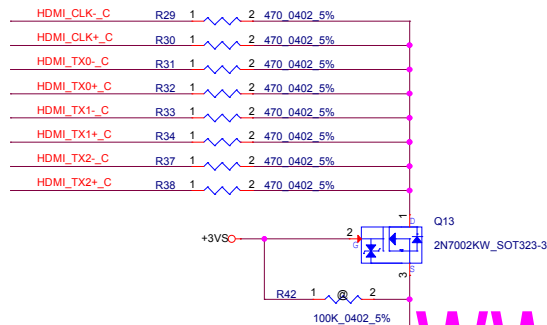
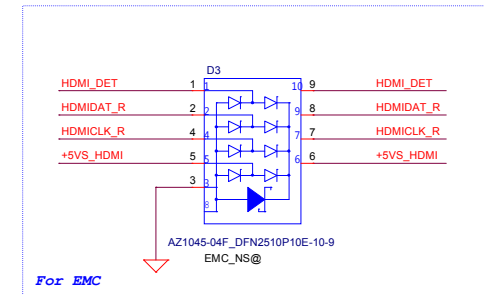
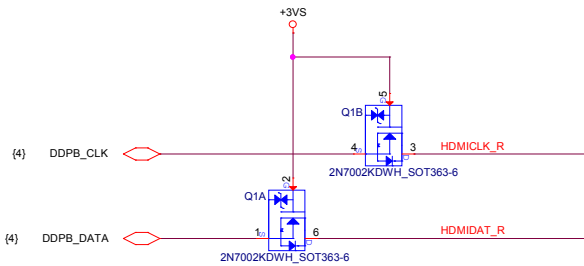
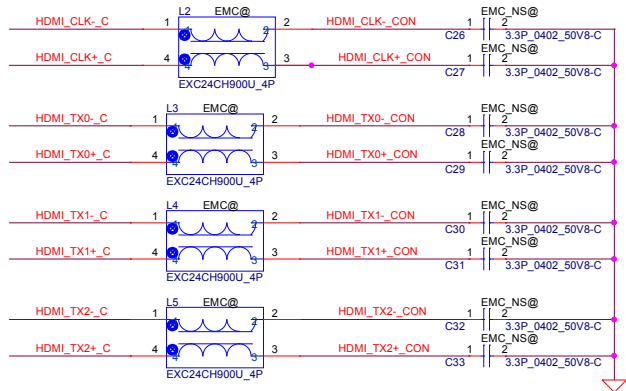


CMOS Camera

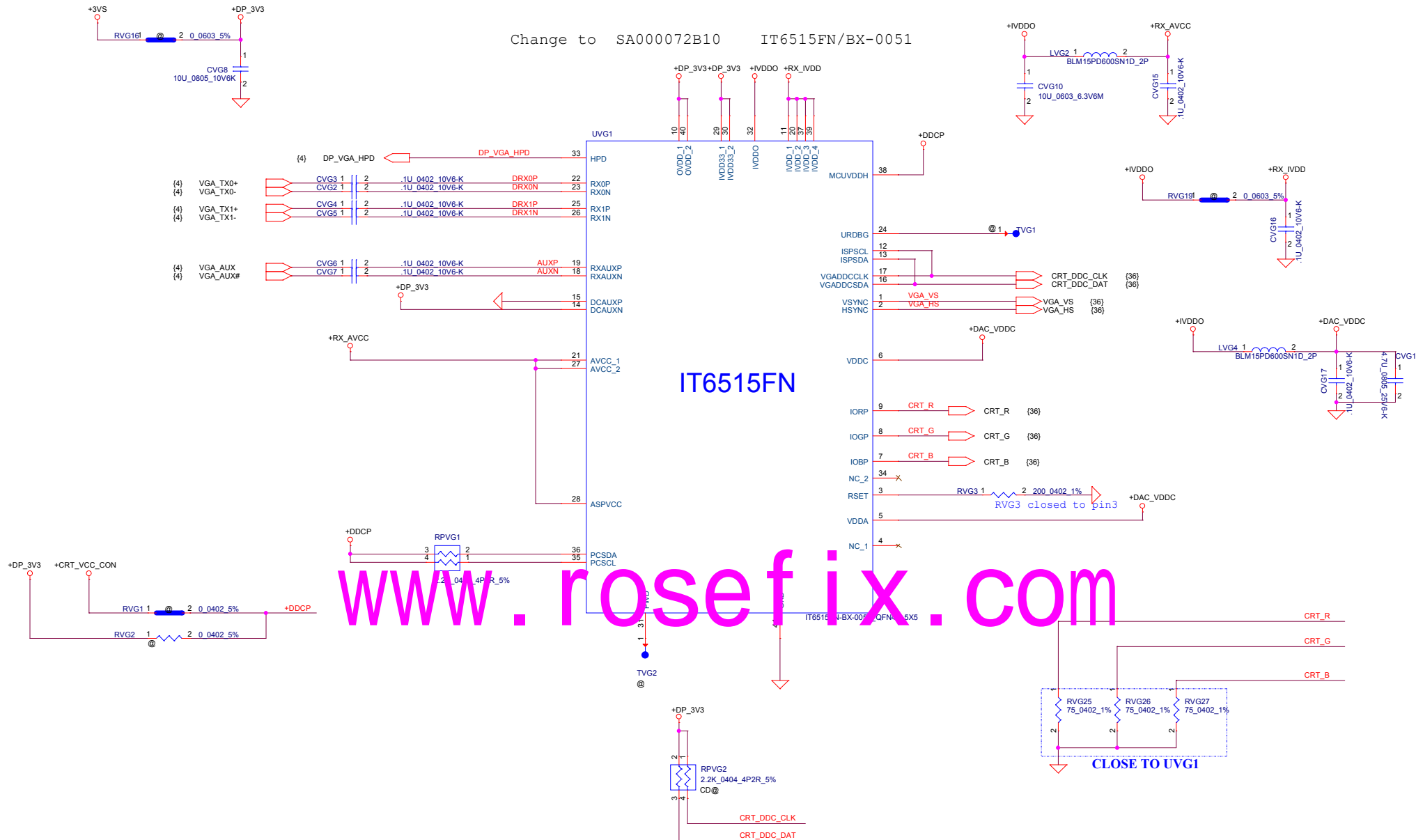


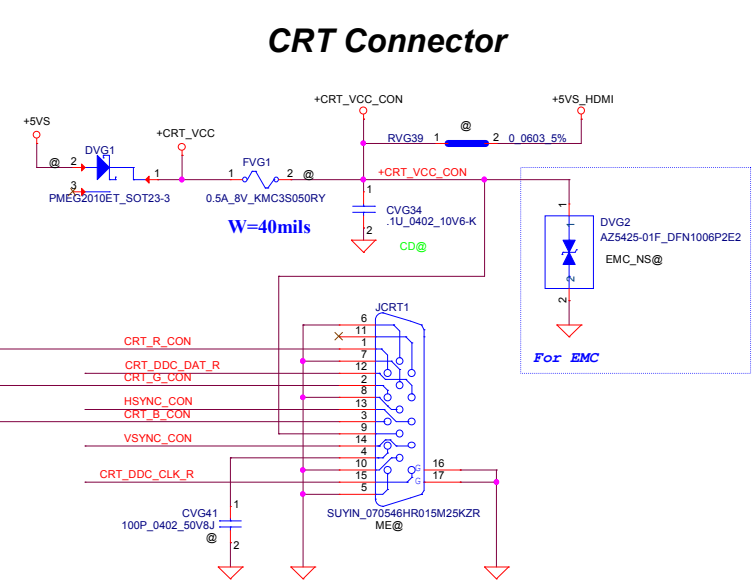
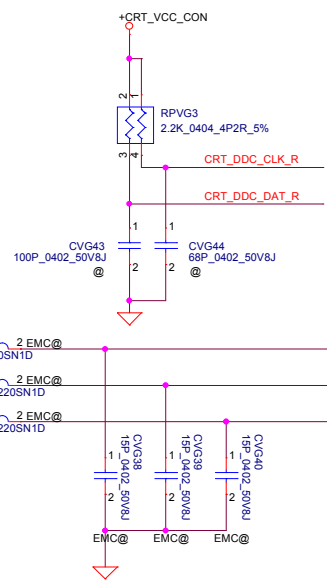
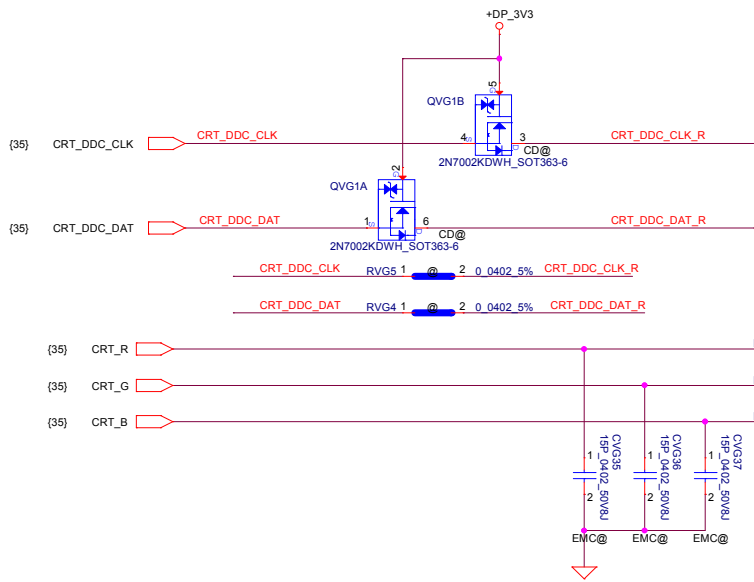
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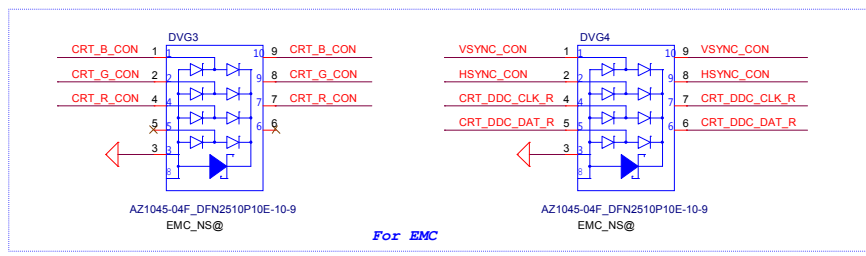
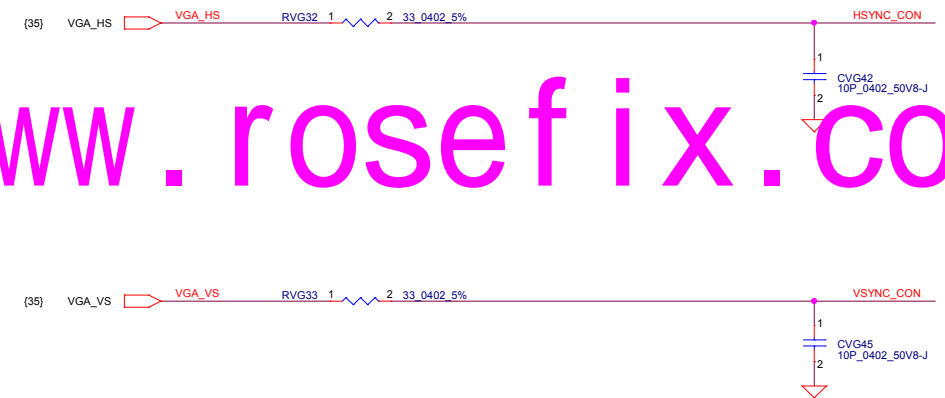


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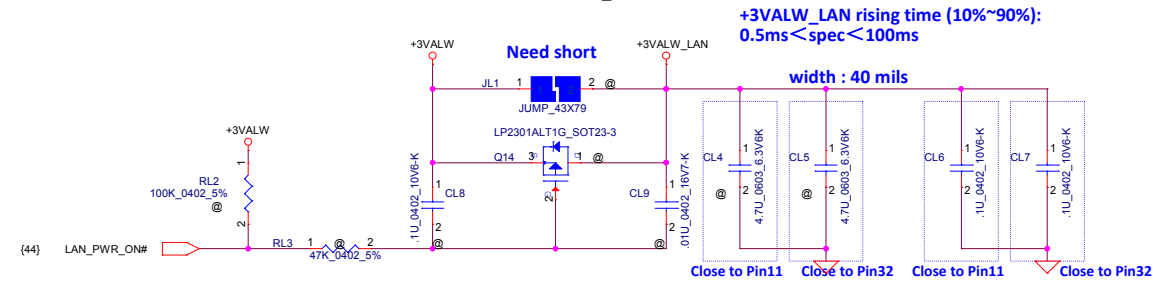




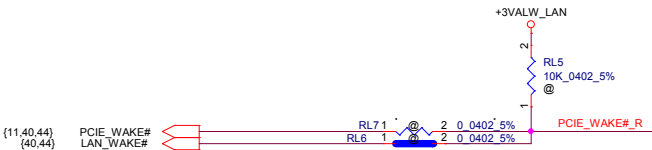
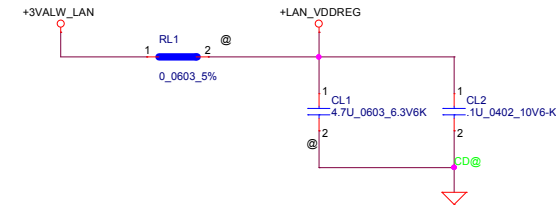
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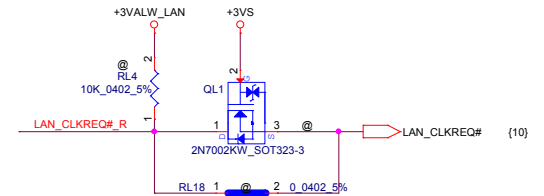
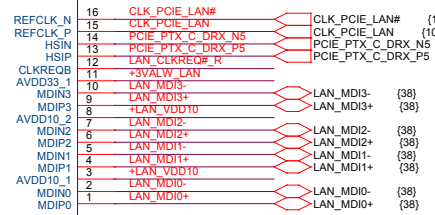
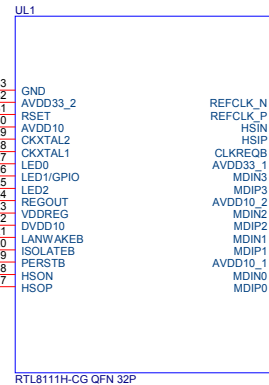
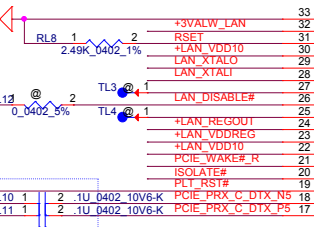
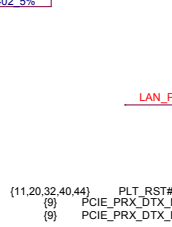
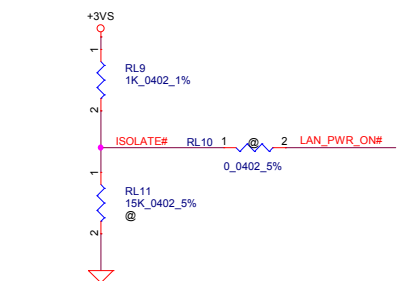
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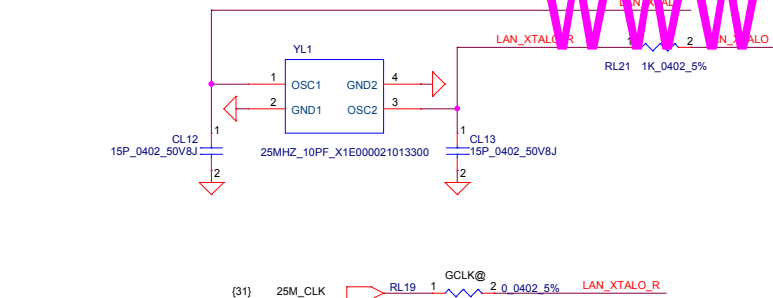
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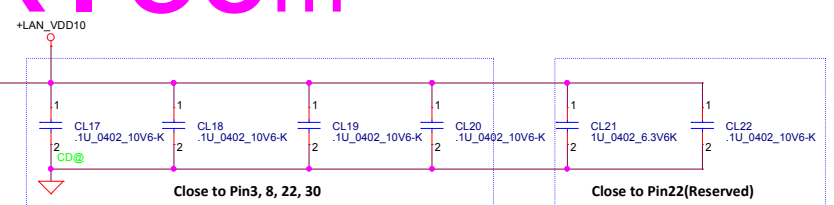
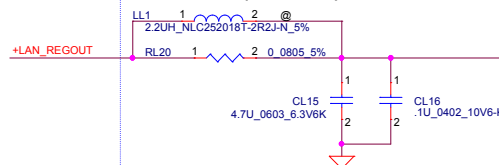
manual change the Codec PN to RTL8111H-CG QFN




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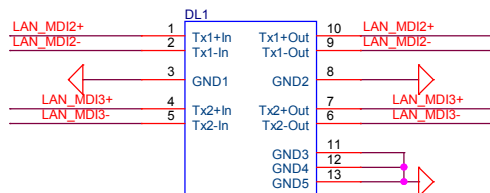
For RTL8111H (LDO mode)



Layout Note: LL1 must be within 200mil to Pin24,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

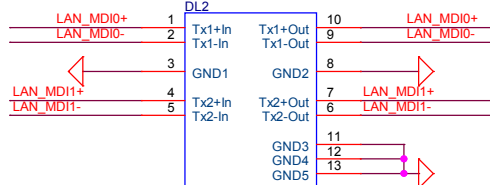
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Size Custom	Document Number	BMWD1			Date: Monday, August 10, 2015
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DL1/DL2
1'S PN:SC400007R00



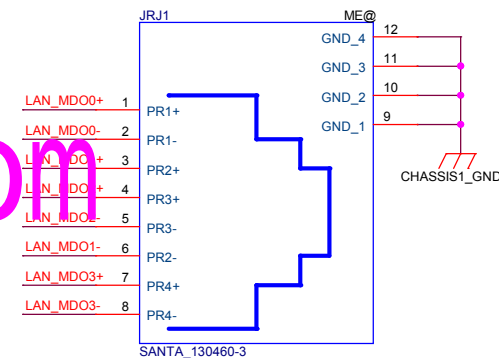
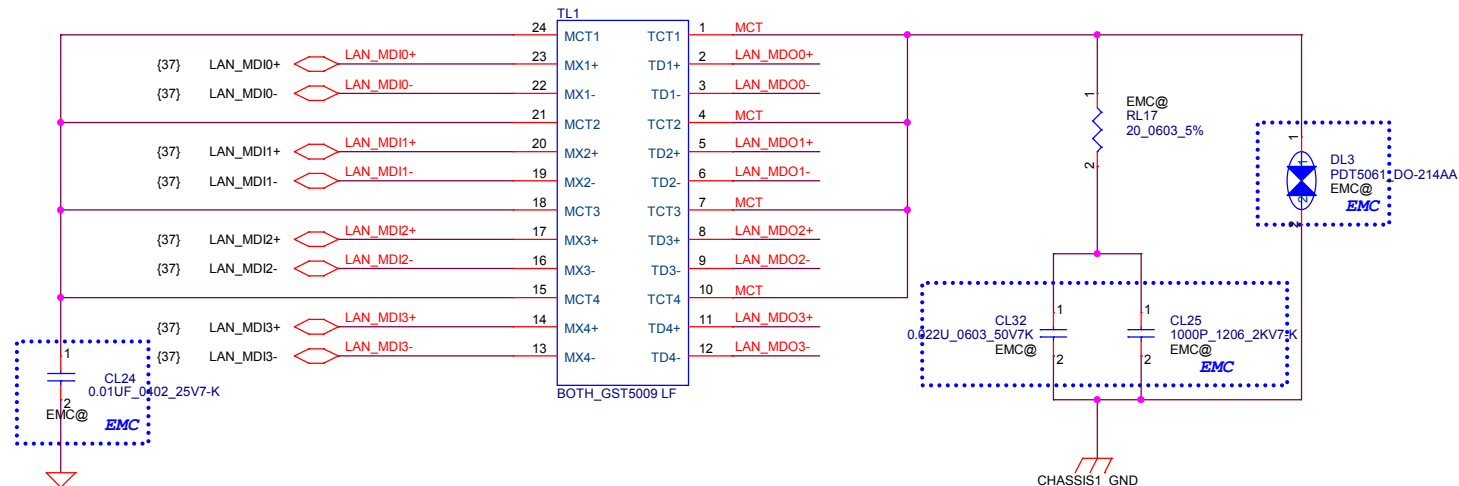
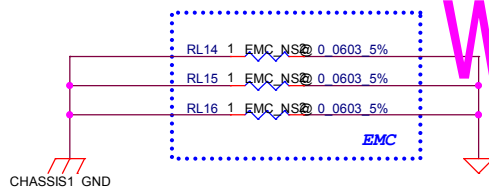
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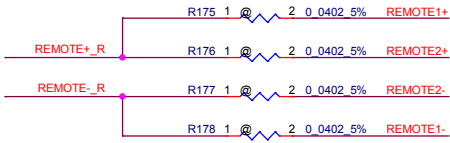
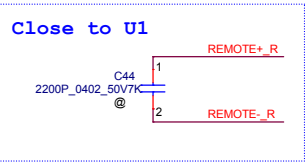
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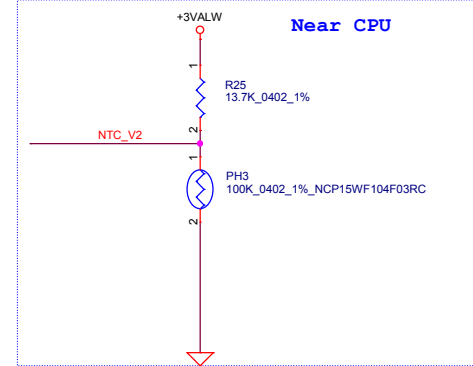
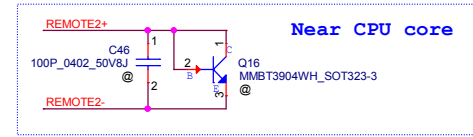
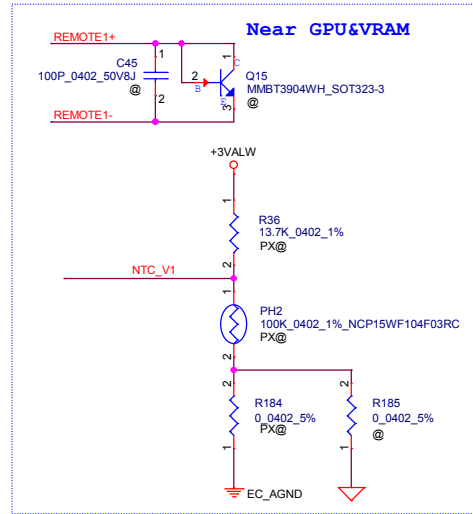
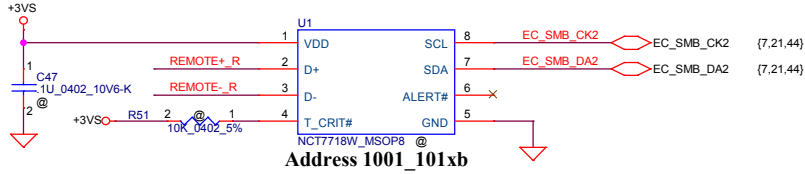
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				3	BMWD1
				Date:	Monday, August 10, 2015
				Sheet	38 of 60
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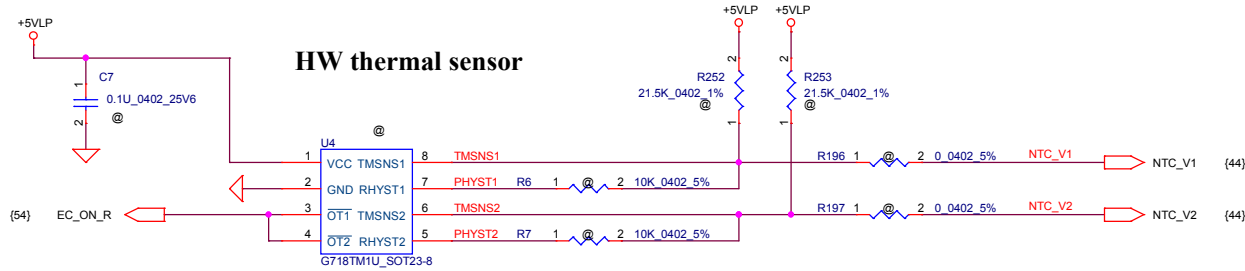


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM



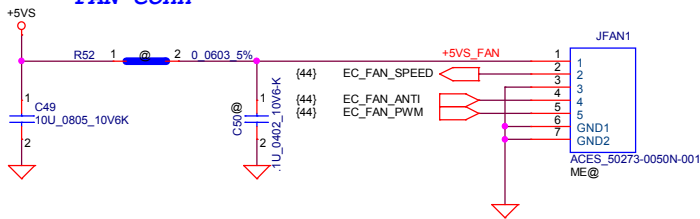
HW thermal sensor



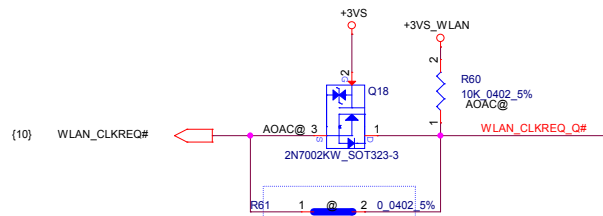
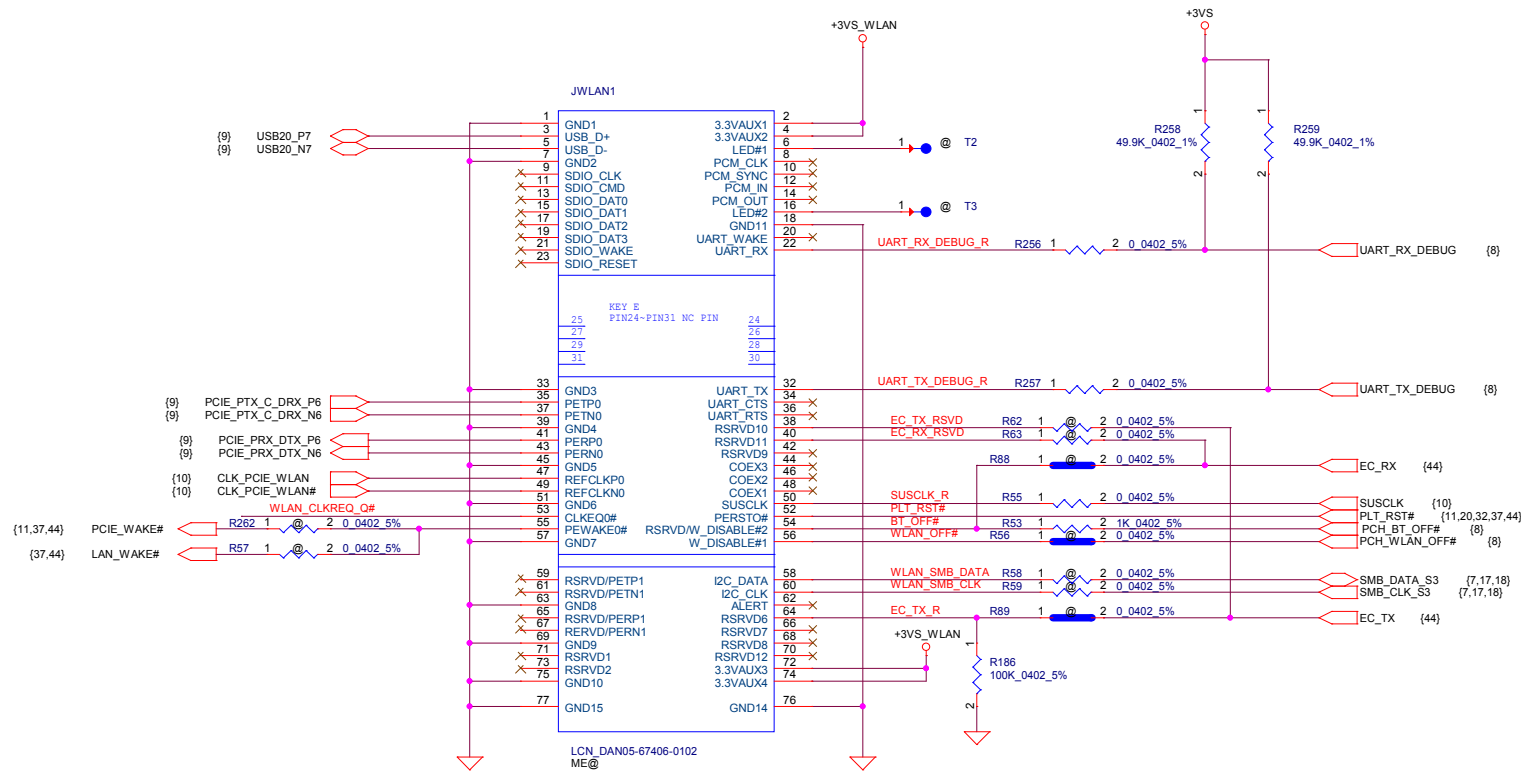
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold:
RHYST=(RSET*RTML) / (3*RT1 - RSET)
56+/-30C

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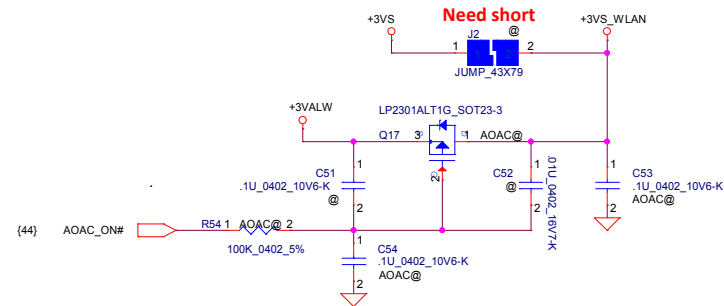
FAN Conn



Mini-Express Card(WLAN/WiMAX)

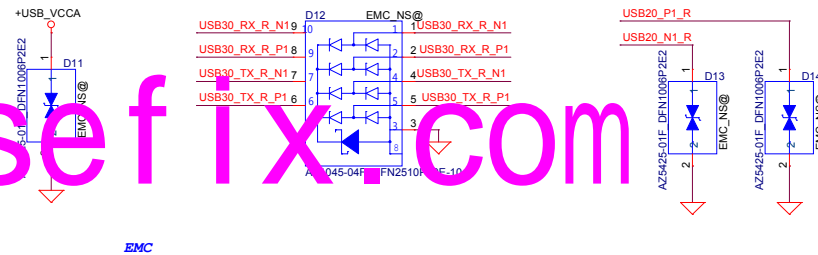
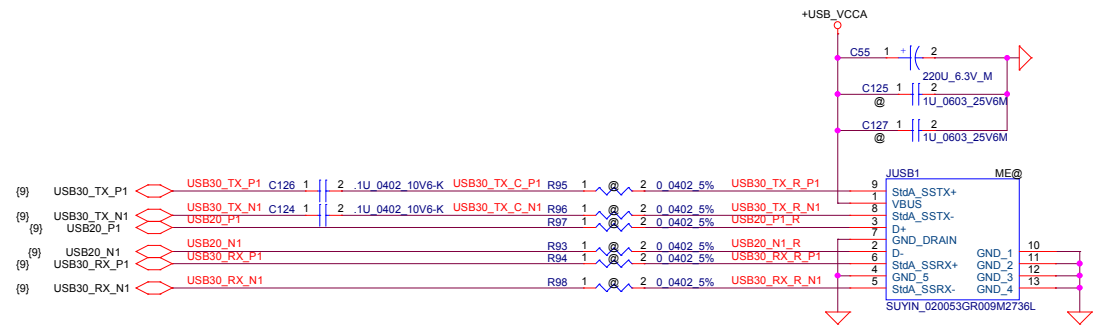
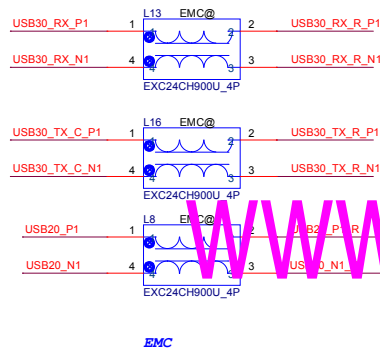
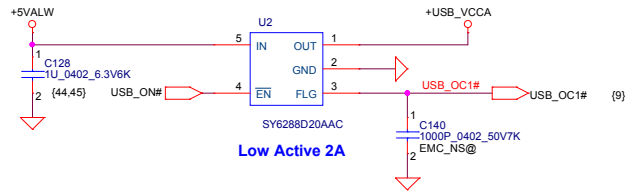


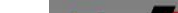
If support AOAC, NC R61;
if not support AOAC, stuff R61.



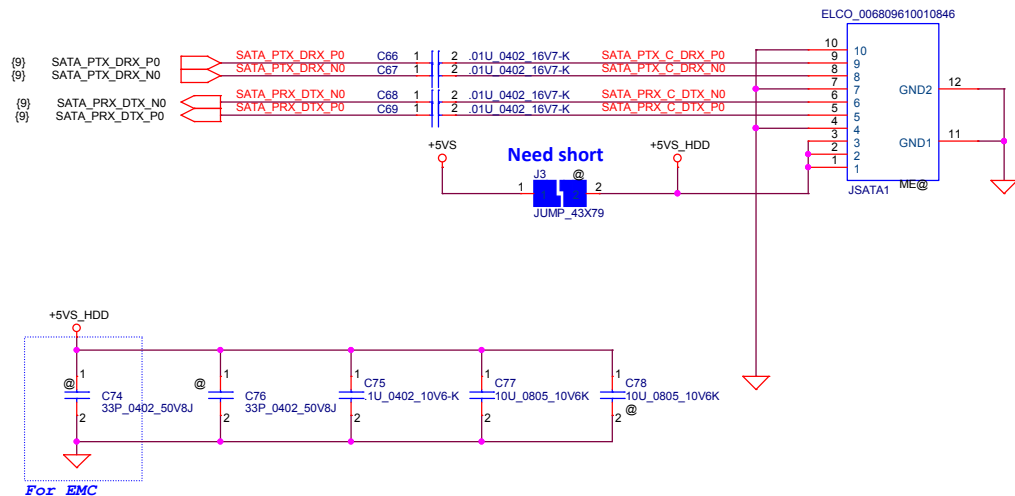
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LEFT SIDE USB3.0 PORT x1

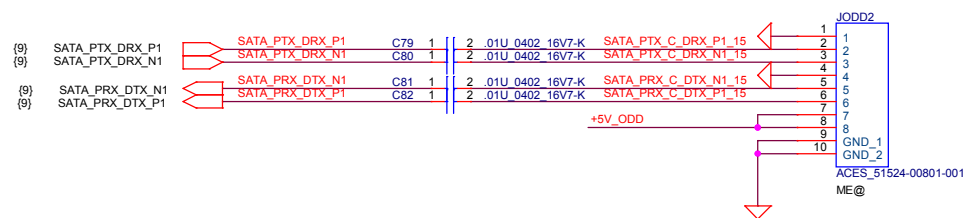


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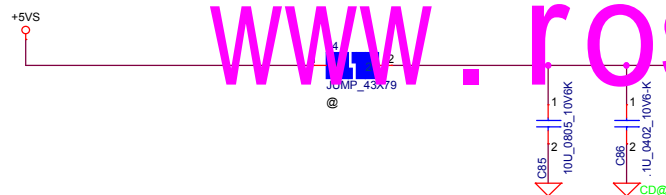
SATA HDD Conn.





SATA ODD FFC Conn

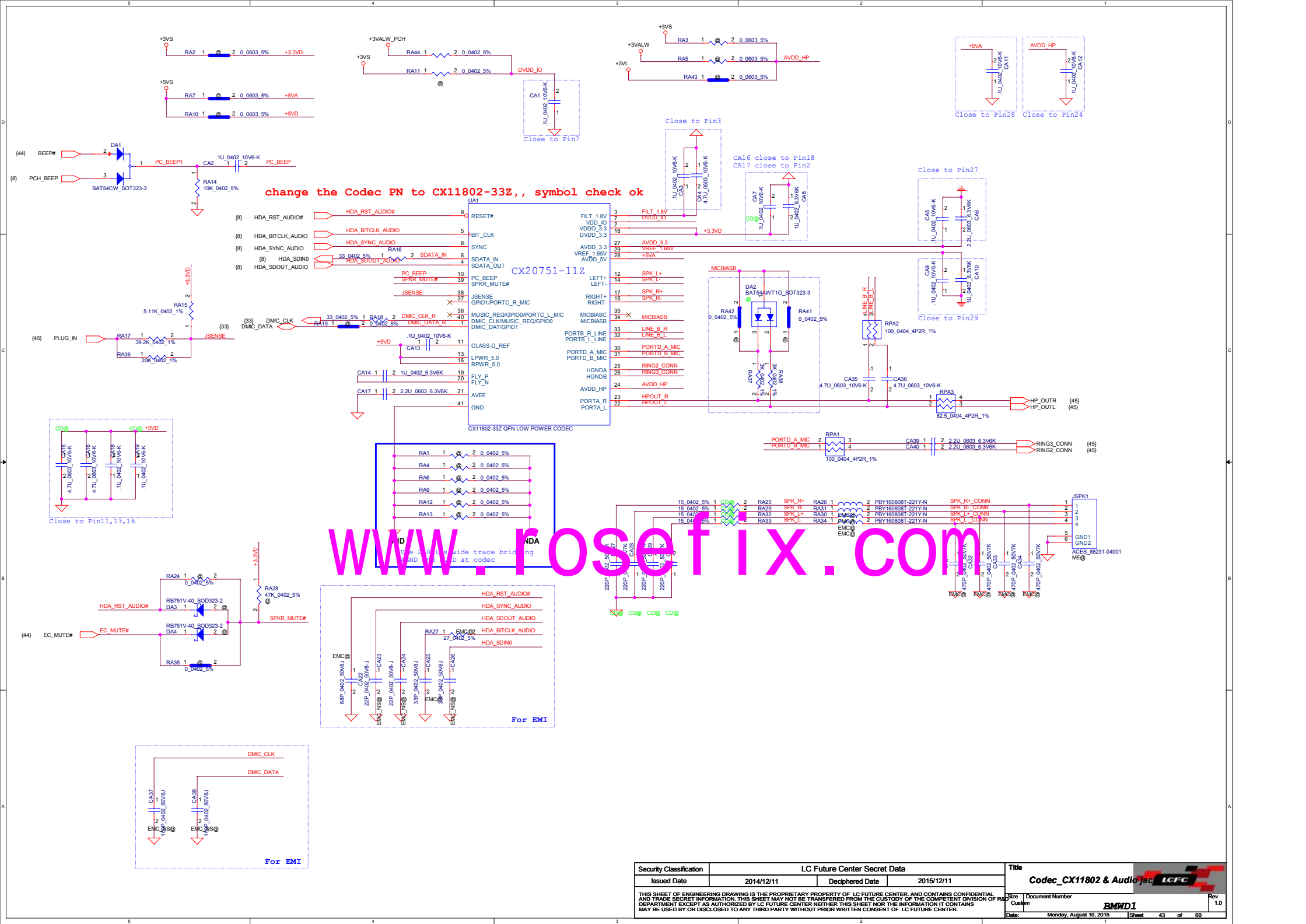


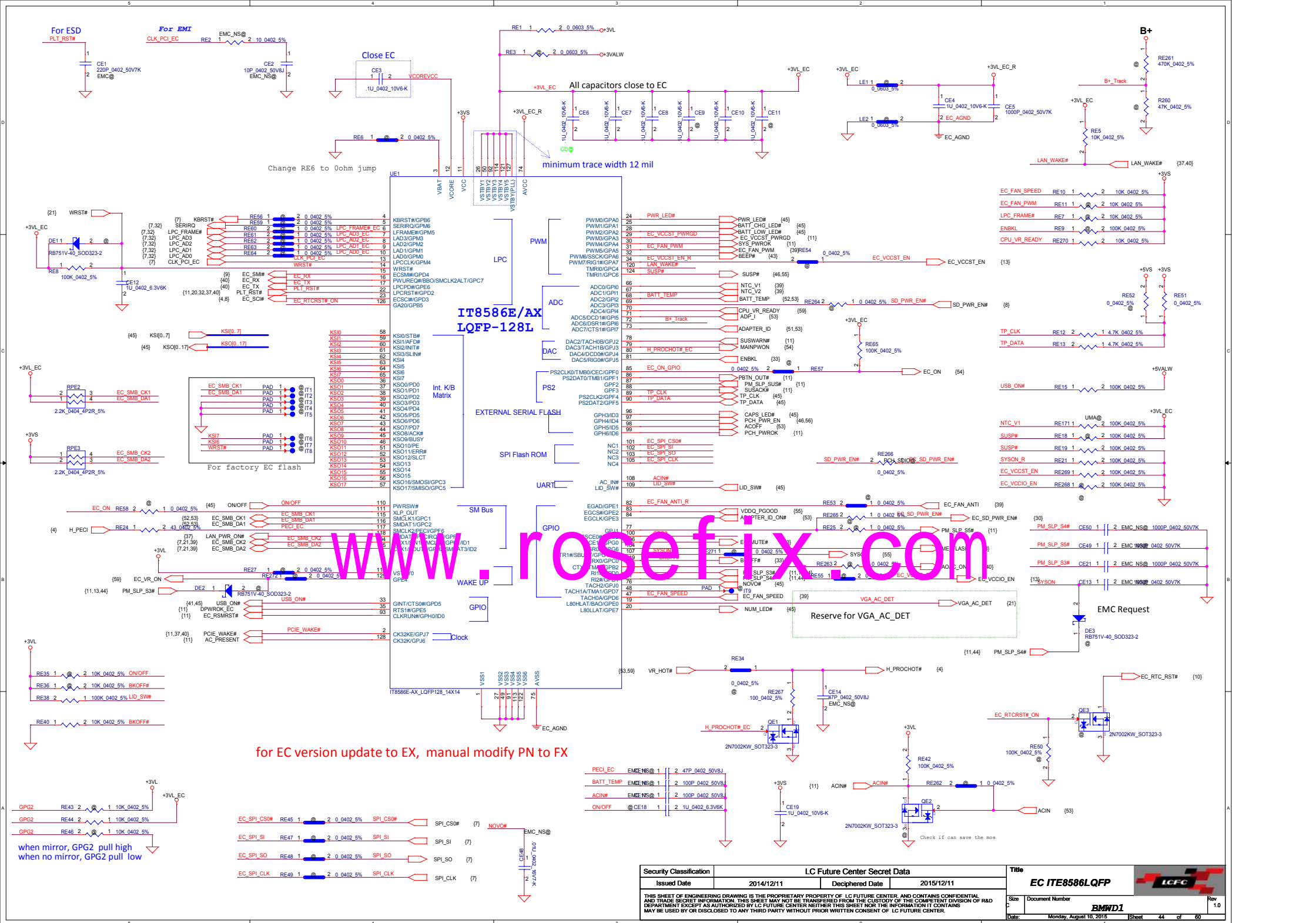
Need Short




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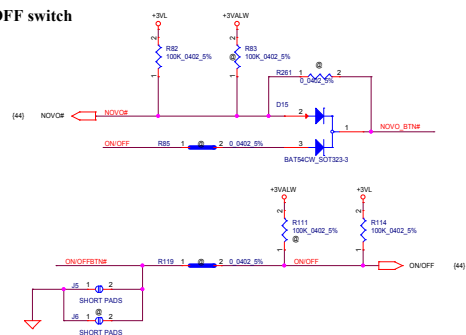
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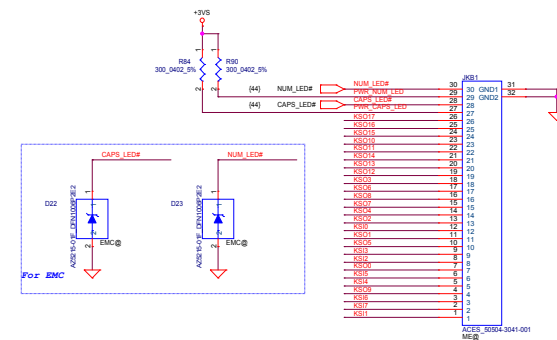
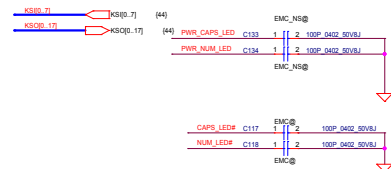


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				BMWD1			
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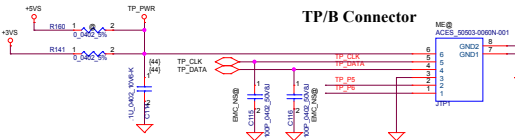
ON/OFF switch



K/B Connector



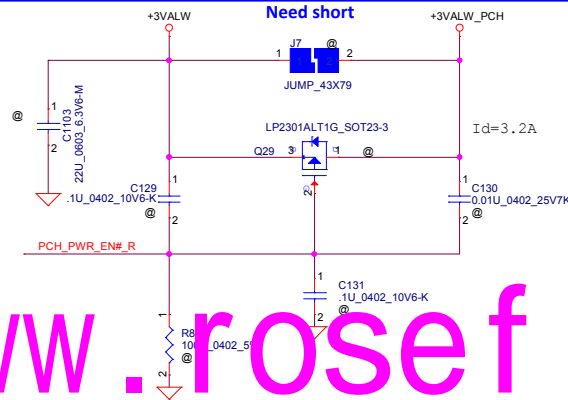
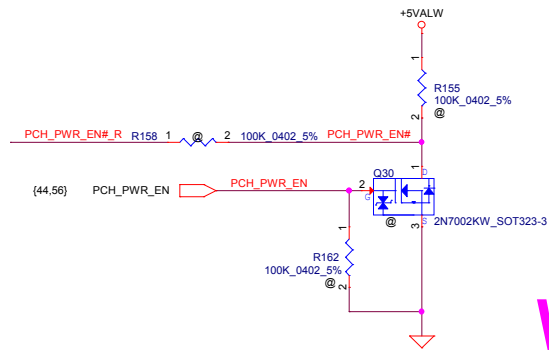
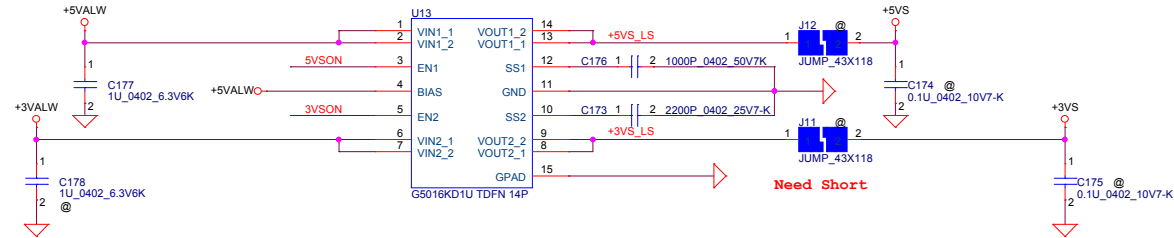
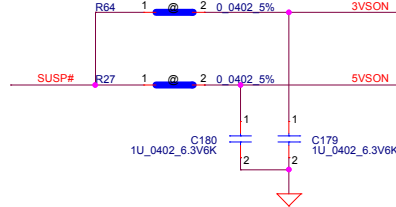
TP/B Connector



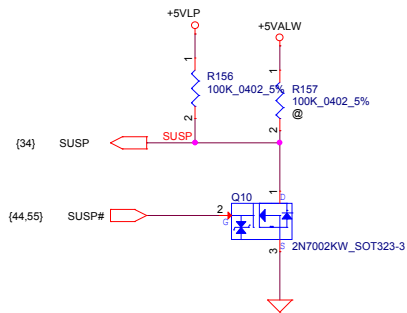
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

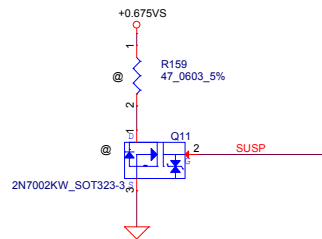
VIN 5V and 3.3V (VBIAS=5V), I_{MAX}(per channel)=6A, R_{DS}=16mohm



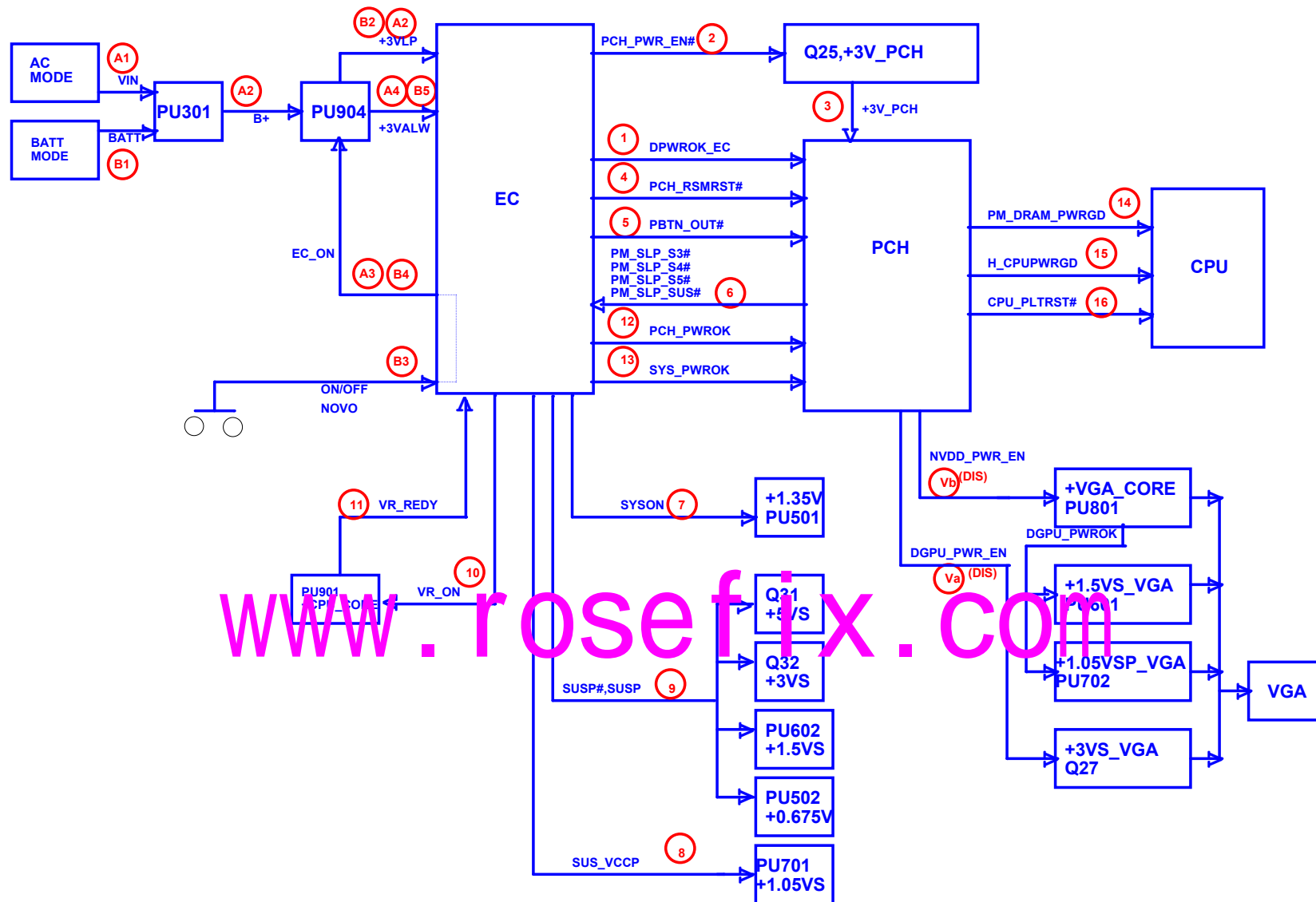
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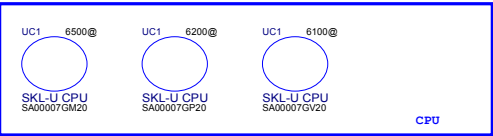
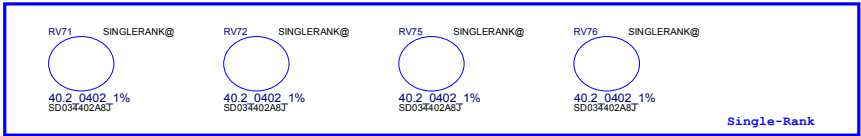
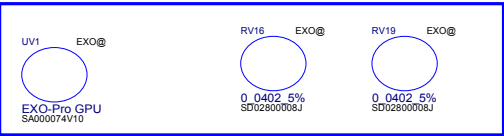


For DisCharge

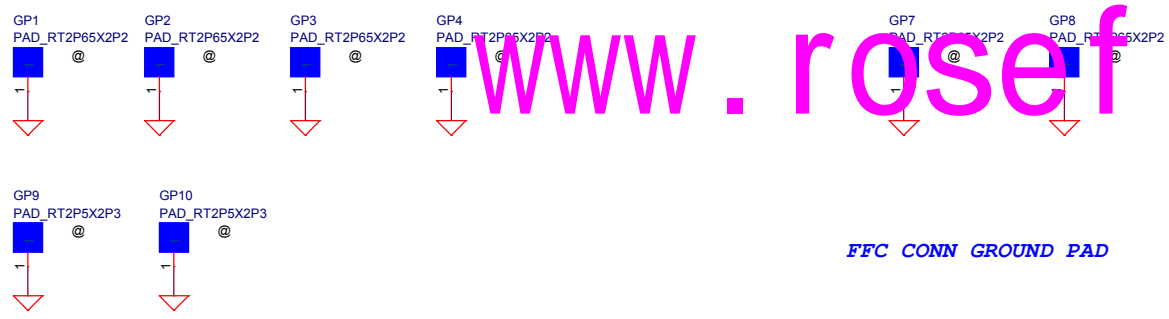
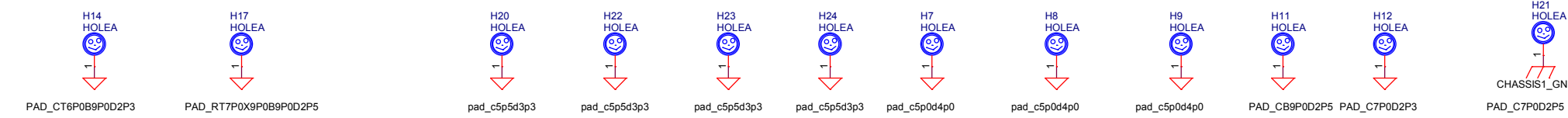
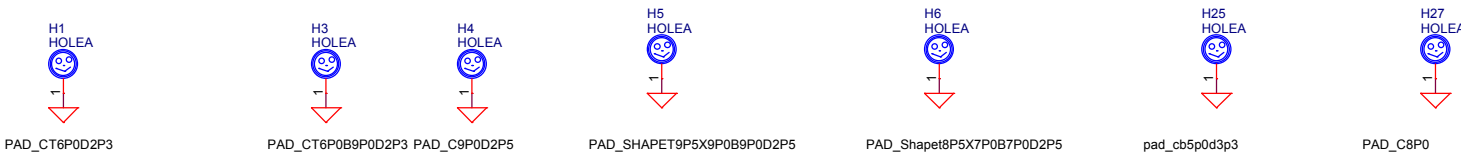
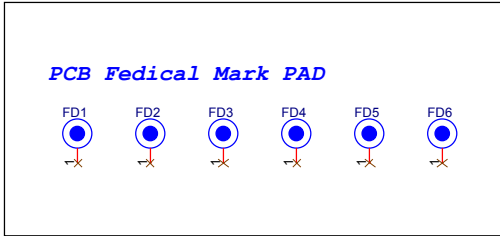


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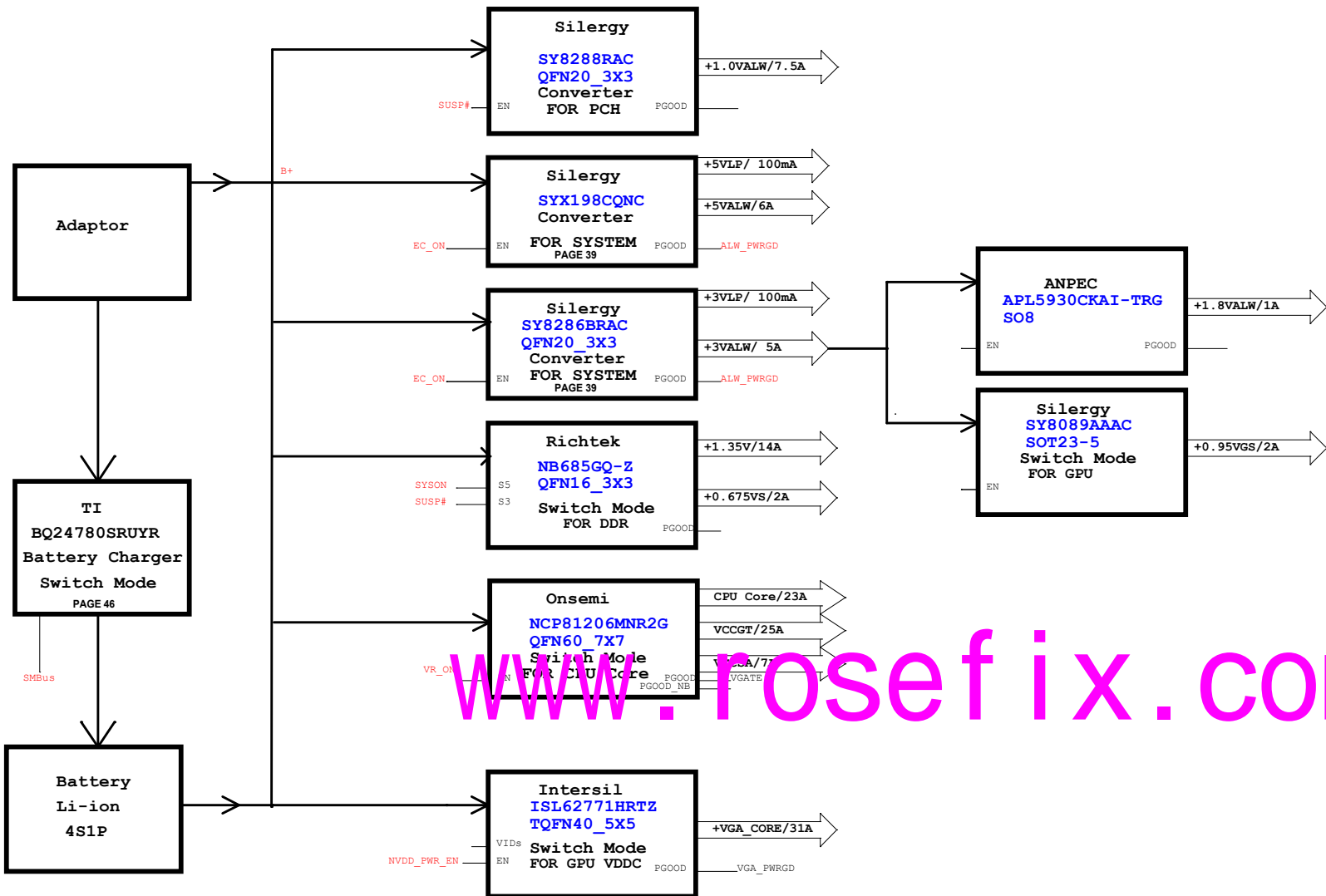
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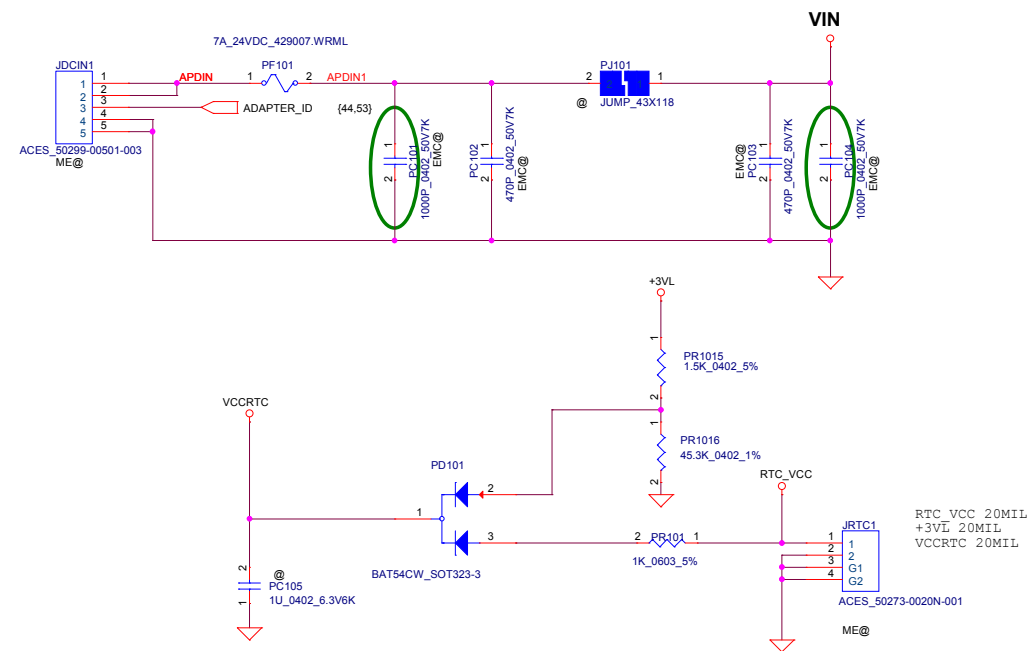
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FFC CONN GROUND PAD

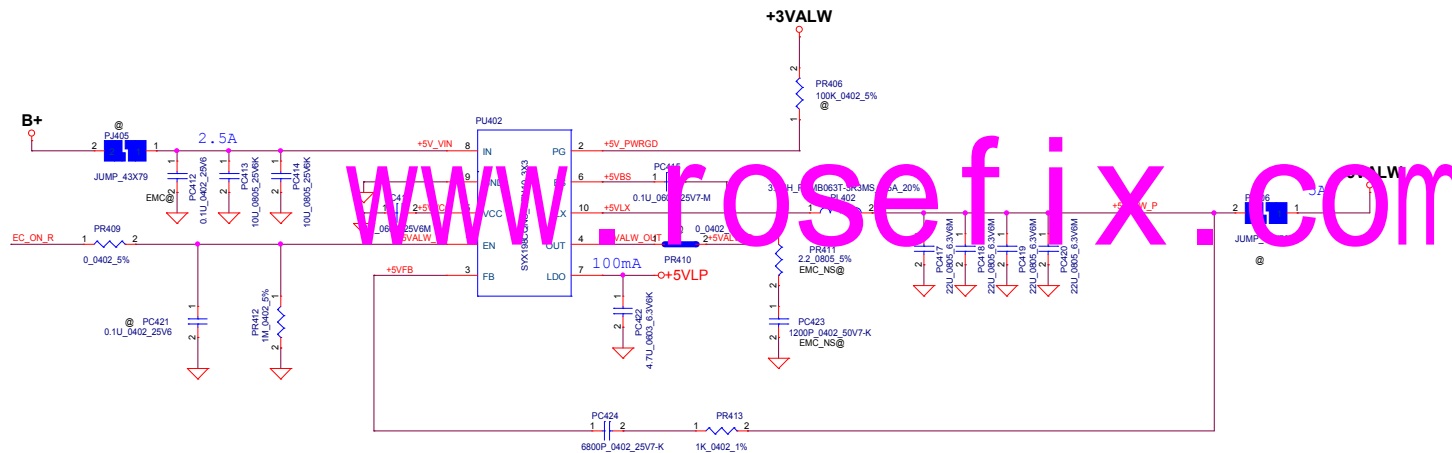
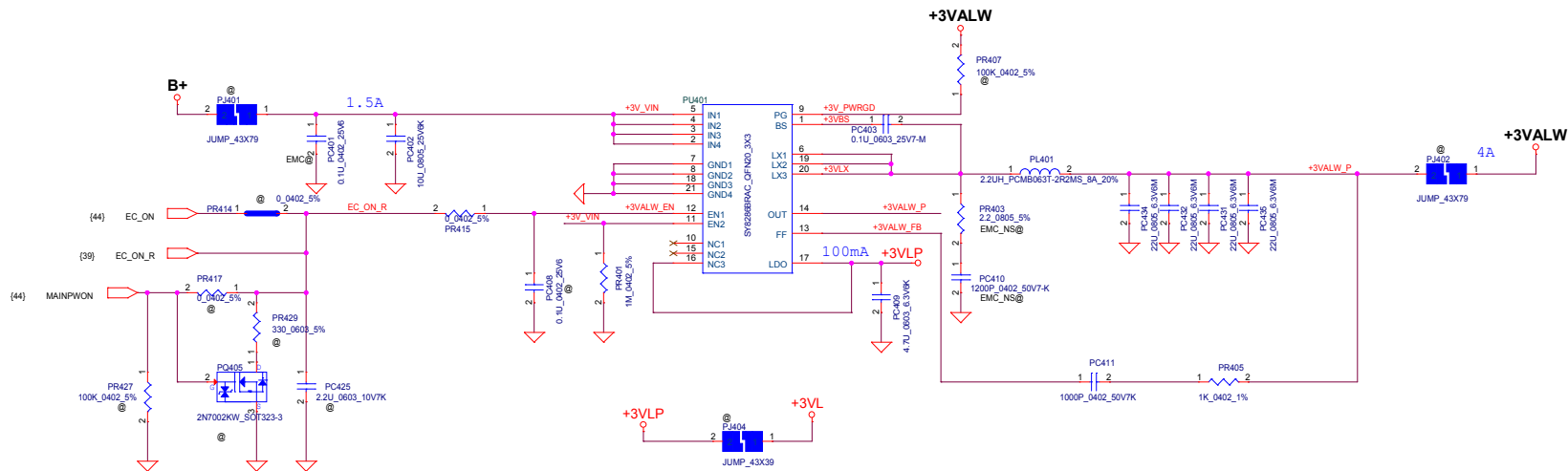
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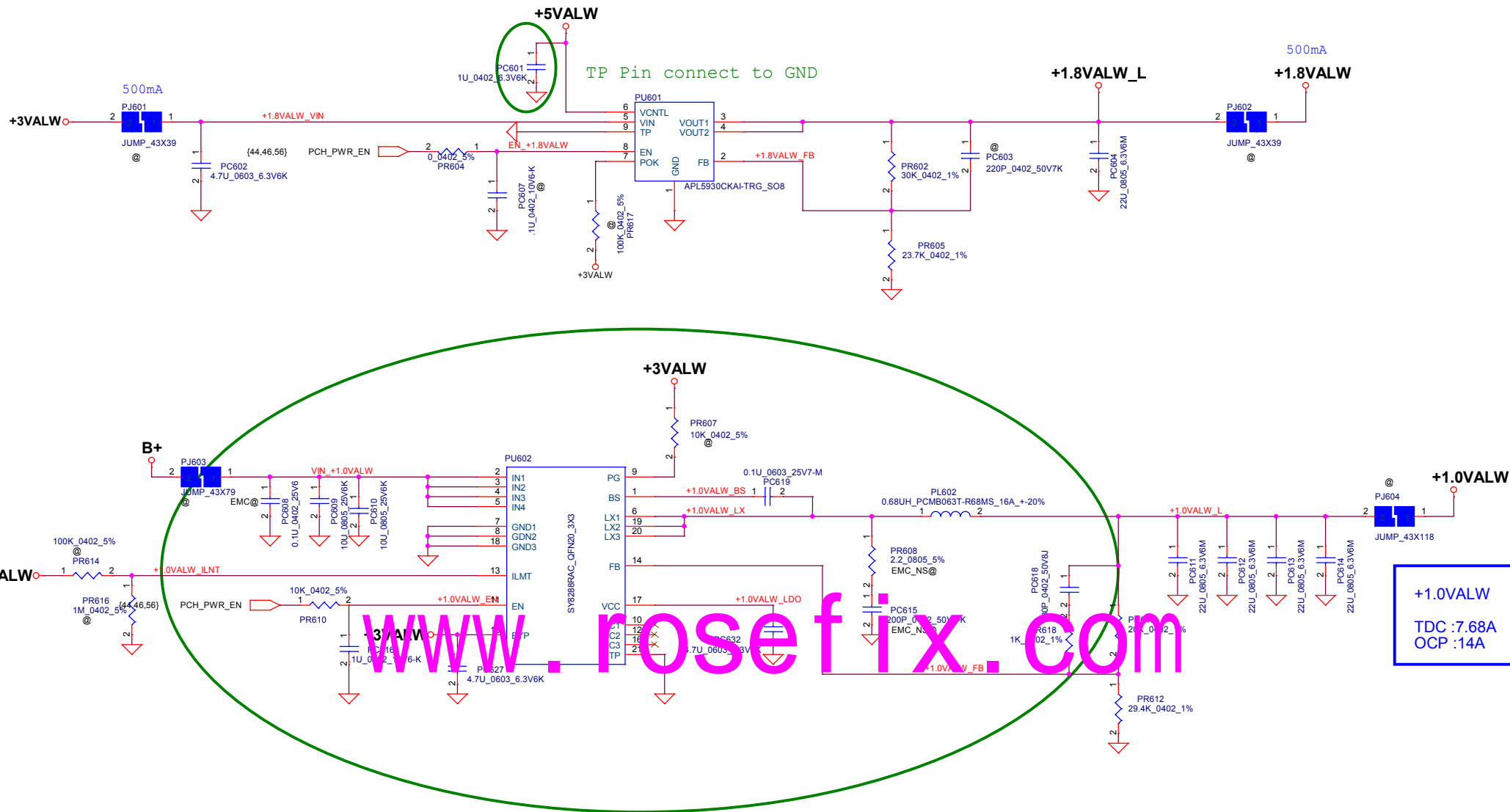
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6800pf soft start 2ms
47nf soft start 7ms

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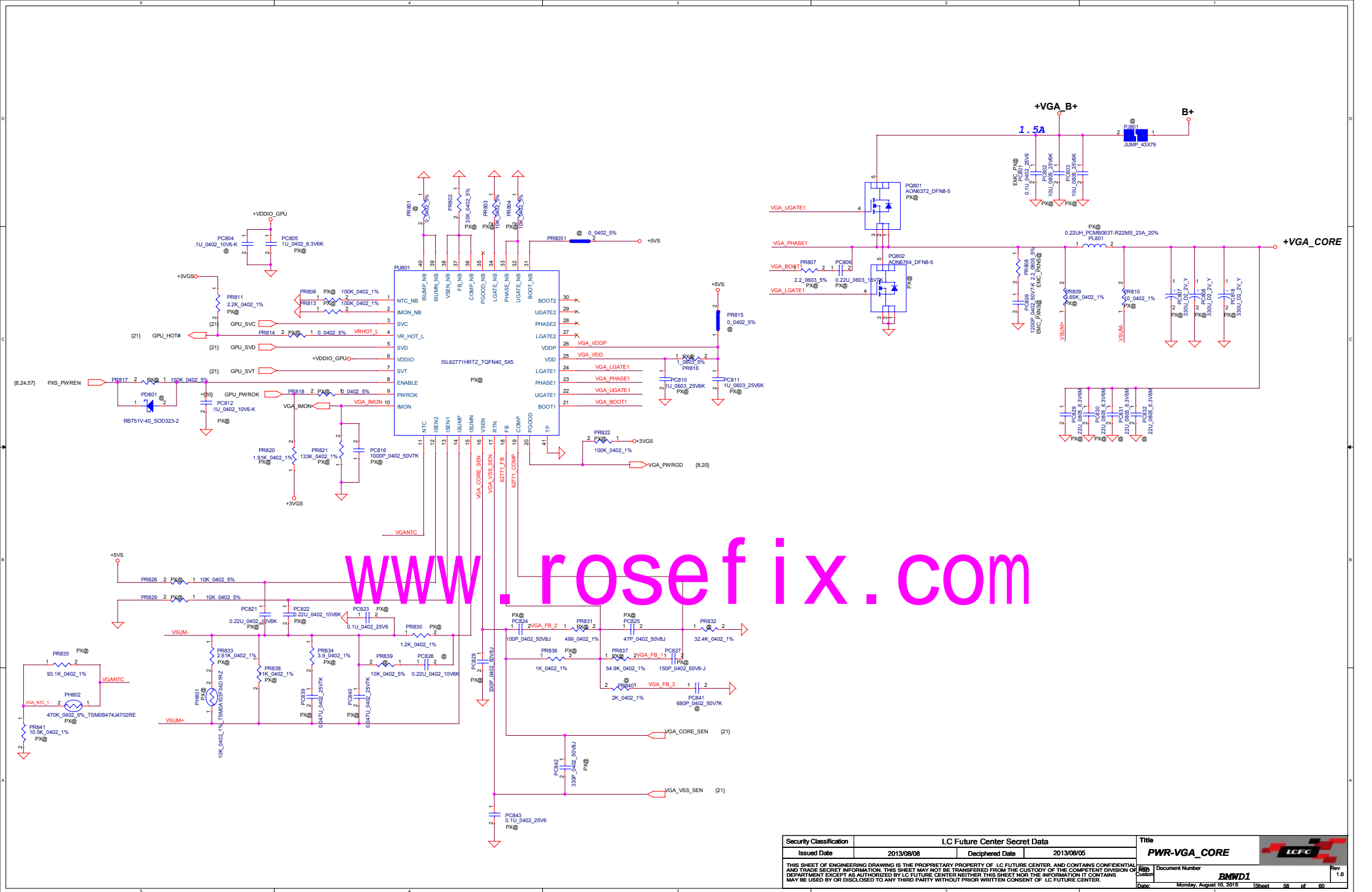



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BMWQ1 & Q2



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